3-Channel Low Power Video Amplifier with I²C Control, Selectable Filters, 6-dB Gain, SAG Correction, 2:1 Input MUX, and Selectable Input Bias Modes

FEATURES

- **3-Video Amplifiers for CVBS, S-Video™, Y'U'V', SD/ED/HD Y'P'$_B$P'$_R$, and G'B'R' (R'G'B')**
- **I²C™ Control of All Functions**
- **Integrated Low-Pass Filters**
  - **Fifth Order Butterworth Characteristics**
  - **Selectable Corner Frequencies of 9-MHz, 16-MHz, 35-MHz, and Bypass (190-MHz)**
- **Selectable Input Bias Modes**
  - **AC-Coupled with Sync-Tip Clamp**
  - **AC-Coupled with Bias**
  - **DC-Coupled with 135-mV Input Shift**
  - **DC-Coupled**
- **2:1 Input MUX Allows Multiple Input Sources**
- **Built-in 6-dB Gain (2V/V)**
- **SAG Correction Capable**
- **2.7-V to 5-V Single Supply Operation**
- **Low 16.6-mA (3.3V) Total Quiescent Current**
- **Individual Disable (0.1 μA) and Mute Control**
- **Rail-to-Rail Output:**
  - **Output Swings within 100 mV from the Rails Which Allows AC or DC Output Coupling**
  - **Able to Drive up to 2 Video Lines – 75 Ω**
- **Low Differential Gain/Phase of: 0.13% / 0.55° at 3.3V**

APPLICATIONS

- **Set Top Box Output Video Buffering**
- **PVR/DVDR Output Buffering**
- **USB/Portable Low Power Video Buffering**

DESCRIPTION

Fabricated using the new complimentary silicon-germanium (SiGe) BiCom-III process, the THS7303 is a low-power, single-supply 2.7-V to 5-V, 3-channel integrated video buffer. It incorporates a selectable 5th order Butterworth filter to eliminate data converter images. The 9-MHz is a perfect choice for SDTV video including composite (CVBS), S-Video, and 480i/576i Y'P'$_B$P'$_R$, and G'B'R' (R'G'B') signals. The 16-MHz filter is ideal for EDTV 480p/576p Y'P'$_B$P'$_R$, G'B'R', and VGA signals. The 35-MHz filter is useful for HDTV 720p/1080i Y'P'$_B$P'$_R$, G'B'R', and SVGA/XGA signals. For 1080p or SXGA/UXGA signals, the filter can be bypassed allowing a 190-MHz bandwidth, 300-V/μs amplifier to buffer the signal.

Each channel of the THS7303 is individually I²C configurable for all functions which makes it flexible for any application. Its rail-to-rail output stage allows for both ac and dc coupling applications. The 6-dB gain along with the built-in SAG correction allows for maximum flexibility as an output video buffer.

The 16.6-mA total quiescent current (55 mW total power) makes the THS7303 an excellent choice for USB powered or portable video applications. While fully disabled, the THS7303 consumes only 0.1 μA making it ideal for energy sensitive applications.

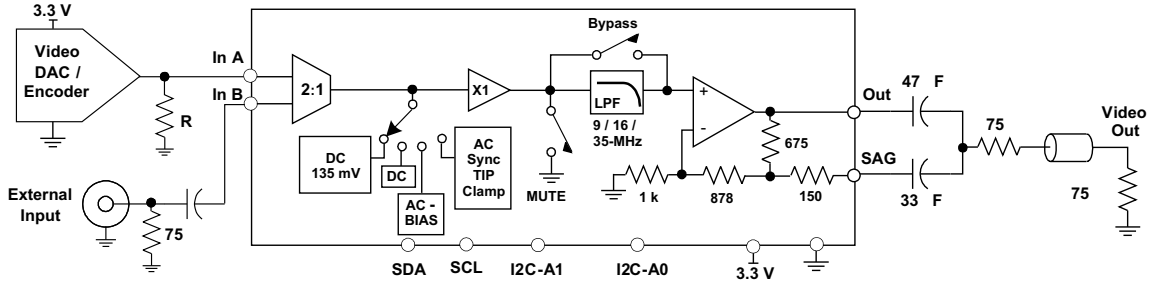


Figure 1. 3.3 V Single-Supply DC-Input/AC-Video Output System w/SAG Correction (1 of 3 Channels Shown)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

As part of the THS7303 flexibility, the 2:1 MUX input can be selected for ac or dc coupled inputs. The ac coupled modes include a sync-tip clamp option for CVBS/Y'/G'/B'/R' with sync or a fixed bias for the C'/P'$_B$/P'$_R$ non-sync channels. The dc input options include a dc input or a dc + 135-mV input offset shift to allow for a full sync dynamic range at the output with 0-V input.

PACKAGING/ORDERING INFORMATION

PACKAGED DEVICES(1)	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
THS7303PW	TSSOP-20	Rails, 75
THS7303PWR		Tape and reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{SS}	Supply voltage, V_{S+} to GND		5.5 V
V_I	Input voltage		–0.4V to V_{S+}
I_O	Output current		±125 mA
	Continuous power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature, any condition(2)		150°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)		125°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
	ESD ratings	HBM	2000 V
		CDM	750 V
		MM	100 V

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1) (T_J = 125°C)	
			T_A = 25°C	T_A = 85°C
TSSOP – 20 (PW)	32.3	83(2)	1.2 W	0.48 W

(1) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and reliability.
(2) This data was taken with the JEDEC High-K test PCB. For the JEDEC low-K test PCB, the θ_{JA} is 125.8°C.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage, V_{S+}	2.7		5	V
T_A	Ambient temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS, V_{S+} = 3.3 V

R_L = 150 Ω to GND, Filter Select = 9 MHz, Input Bias = DC, SAG pin shorted to the output pin (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
AC PERFORMANCE							
Small-signal bandwidth (–3 dB) V_O– 0.2 V_{PP}	Filter Select = 9 MHz(1)	9	7.6/10.4	7.4/10.6	7.3/10.7	MHz	Min/Max
	Filter Select = 16 MHz(1)	16	13.4/18.6	13.1/18.9	13/19	MHz	Min/Max
	Filter Select = 35 MHz(1)	35	29.4/40.6	29.1/40.9	29/41	MHz	Min/Max
	Filter Select = Bypass	175				MHz	
Large-signal bandwidth (–3 dB) V_O– 2 V_{PP}	Filter Select = 9 MHz	9				MHz	
	Filter Select = 16 MHz	16				MHz	
	Filter Select = 35 MHz	35				MHz	
	Filter Select = Bypass	83				MHz	
Slew rate	Filter Select = Bypass: Vo = 2Vpp	300				V/µs	
Group delay at 100 kHz	Filter Select = 9 MHz	54				ns	
	Filter Select = 16 MHz	31.5				ns	
	Filter Select = 35 MHz	17				ns	
	Filter Select = Bypass	3				ns	
Group delay variation with respect to 100 kHz	Filter Select = 9 MHz: at 5.1 MHz	10.5				ns	
	Filter Select = 16 MHz: at 11 MHz	8				ns	
	Filter Select = 35 MHz: at 27 MHz	4.8				ns	
Group delay matching	All filters: channel-to-channel	0.5				ns	
Attenuation with respect to 100 kHz	Filter Select = 9 MHz: at 5.75 MHz	0.2	-0.3/0.9	-0.5/1.1	-0.6/1.2	dB	Min/Max
	Filter Select = 9 MHz: at 27 MHz	43	33	32	31	dB	Min
	Filter Select = 16 MHz: at 11 MHz	0.25	-0.3/0.9	-0.5/1.1	-0.6/1.2	dB	Min/Max
	Filter Select = 16 MHz: at 54 MHz	44	33	32	31	dB	Min
	Filter Select = 35 MHz: at 27 MHz	0.7	-0.3/2.7	-0.5/2.8	-0.6/2.9	dB	Min/Max
	Filter Select = 35 MHz: at 74 MHz	28	15	14	13	dB	Min
Mute feed through	Filter Select = Bypass: at 30 MHz	-73				dB	
Differential gain	Filter Select = 9 MHz: NTSC/PAL	0.13%/0.27%					
Differential phase	Filter Select = 9 MHz: NTSC/PAL	0.55°/0.65°					
Total harmonic distortion f = 1 MHz, 2 V_{PP}	Filter Select = 9 MHz	–59				dB	
	Filter Select = 16 MHz	–62				dB	
	Filter Select = 35 MHz	–58				dB	
	Filter Select = Bypass	–60				dB	
Signal to noise ratio (unified weighting per CCIR 576-2 reommendation)	Filter Select = 9 MHz, 480i source	84				dB	
	Filter Select = 16 MHz, 480p source	82				dB	
	Filter Select = 35 MHz, 720p source	79				dB	
	Filter Select = Bypass(2), 720p source	67				dB	
Channel-to-Channel Crosstalk (V_O = 2 V_{PP})	Filter Select = 9 MHz: at 1 MHz	–65				dB	
	Filter Select = 16 MHz: at 1 MHz	–67				dB	
	Filter Select = 35 MHz: at 1 MHz	–69				dB	
	Filter Select = Bypass: at 1 MHz	–70				dB	

(1) The Min/Max values listed are specified by design only. PCB capacitance affects the filter characteristics, especially the 35-MHz and bypass mode responses.
(2) Bandwidth up to 100-MHz, No Weighting, Tilt Null

ELECTRICAL CHARACTERISTICS, V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND, Filter Select = 9 MHz, Input Bias = DC, SAG pin shorted to the output pin (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
MUX Isolation	Filter Select = 9 MHz: at 5.1 MHz	70				dB	
	Filter Select = 16 MHz: at 11 MHz	69				dB	
	Filter Select = 35 MHz: at 27 MHz	69				dB	
	Filter Select = Bypass: at 60 MHz	73				dB	
AC gain – All channels	f = 100 kHz	6	5.7/6.3	5.65/6.35	5.65/6.35	dB	Min/Max
Output impedance	f = 10 MHz	0.7				Ω	
DC PERFORMANCE							
Output offset voltage	Bias = dc	35	90	95	95	mV	Max
Average offset voltage drift	Bias = dc				20	µV/°C	
Bias output voltage	Bias = dc + 135 mV, V_I = 0 V	290	235/345	215/360	200/375	mV	Min/Max
	Bias = ac	1.65	1.5/1.8	1.45/1.85	1.45/1.85	V	Min/Max
Sync tip clamp output voltage	Bias = ac STC	290	210/370	200/380	195/385	mV	Min/Max
Input bias current	Bias = dc - implies Ib out of the pin	–0.6	–4	–5	–5	µA	Max
Average bias current drift	Bias = dc				10	nA/°C	
Sync tip clamp bias current	Bias = ac STC, low bias	1.8	0.6/3.3	0.5/3.5	0.4/3.6	µA	Min/Max
	Bias = ac STC, mid bias	5.8	4.3/8.2	4.1/8.4	4/8.5	µA	Min/Max
	Bias = ac STC, high bias	7.8	6.2/10.8	6/11	5.9/11.1	µA	Min/Max
INPUT CHARACTERISTICS							
Input voltage range	Bias = dc - limited by output	0/1.57	0/1.52	0/1.47	0/1.47	V	Min/Max
Input resistance	Bias = ac bias mode	19				kΩ	
	Bias = dc, dc + 135 mV, ac STC	3				MΩ	
Input capacitance		2				pF	
OUTPUT CHARACTERISTICS							
High output voltage swing	R_L = 150 Ω to midrail	3.15	2.9	2.8	2.8	V	Min
	R_L = 150 Ω to GND	3.05	2.85	2.75	2.75	V	Min
	R_L = 75 Ω to midrail	3.05	2.8	2.7	2.7	V	Min
	R_L = 75 Ω to GND	2.9	2.65	2.55	2.55	V	Min
Low output voltage swing	R_L = 150 Ω to midrail	0.14	0.24	0.27	0.28	V	Max
	R_L = 150 Ω to GND	0.09	0.17	0.2	0.21	V	Max
	R_L = 75 Ω to GND	0.24	0.33	0.36	0.37	V	Max
	R_L = 75 Ω to GND	0.09	0.17	0.2	0.21	V	Max
Output current	R_L = 10 Ω to midrail, sourcing	70	45	42	40	mA	Min
	R_L = 10 Ω to midrail, sinking	70	45	42	40	mA	Min
POWER SUPPLY							
Maximum operating voltage		3.3	5.5	5.5	5.5	V	Max
Minimum operating voltage		3.3	2.6	2.6	2.6	V	Min
Maximum quiescent current	Per channel V_I = 200 mV	6	7.2	7.4	7.5	mA	Max
Minimum quiescent current	Per channel V_I = 200 mV	6	4.8	4.6	4.5	mA	Min
Total quiescent current	All channels ON, V_I = 200 mV(3)	16.6				mA	
Power supply rejection (+PSRR)	V_{S+} = 3.5 V to 3.1 V	62	37	35	35	dB	Min

(3) Due to sharing of internal bias currents, the quiescent current, with all channels operating, is less than the single individual channel quiescent currents added together.

ELECTRICAL CHARACTERISTICS, V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND, Filter Select = 9 MHz, Input Bias = DC, SAG pin shorted to the output pin (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	−40°C to 85°C	UNITS	MIN/MAX
DISABLE CHARACTERISTICS							
Quiescent current	All 3 channels disabled (4)	0.1				µA	
Turn-on time delay (t_{ON})	Time reaches 50% of final value after I^2C control is completed	5				µs	
Turn-on time delay (t_{OFF})		2				µs	

(4) Note that the I^2C circuitry is still active while in Disable mode. The current shown is while there is no activity with the THS7303's I^2C circuitry.

ELECTRICAL CHARACTERISTICS, V_{S+} = 5 V

R_L = 150 Ω to GND, Filter Select = 9 MHz, Input Bias = dc, SAG pin shorted to the output pin (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
AC PERFORMANCE							
Small-signal bandwidth (–3 dB) V_O– 0.1 V_{PP}	Filter Select = 9 MHz(1)	9	7.6/10.4	7.4/10.6	7.3/10.7	MHz	Min/Max
	Filter Select = 16 MHz(1)	16	13.4/18.6	13.1/18.9	13/19	MHz	Min/Max
	Filter Select = 35 MHz(1)	35	29.4/40.6	29.1/40.9	29/41	MHz	Min/Max
	Filter Select = Bypass	190				MHz	
Large-signal bandwidth (–3 dB) V_O– 2 V_{PP}	Filter Select = 9 MHz	9				MHz	
	Filter Select = 16 MHz	16				MHz	
	Filter Select = 35 MHz	35				MHz	
	Filter Select = Bypass	90				MHz	
Slew rate	Filter Select = Bypass	320				V/µs	
Group delay at 100 kHz	Filter Select = 9 MHz	53				ns	
	Filter Select = 16 MHz	31				ns	
	Filter Select = 35 MHz	16.5				ns	
	Filter Select = Bypass	2.9				ns	
Group delay variation with respect to 100 kHz	Filter Select = 9 MHz: at 5.1 MHz	10.5				ns	
	Filter Select = 16 MHz: at 11 MHz	7.5				ns	
	Filter Select = 35 MHz: at 27 MHz	4.5				ns	
Group delay matching	All filters: channel-to-channel	0.5				ns	
Attenuation with respect to 100 kHz	Filter Select = 9 MHz: at 5.75 MHz	0.2	-0.3/0.9	-0.5/1.1	-0.6/1.2	dB	Min/Max
	Filter Select = 9 MHz: at 27 MHz	42	33	32	31	dB	Min
	Filter Select = 16 MHz: at 11 MHz	0.25	-0.3/0.9	-0.5/1.1	-0.6/1.2	dB	Min/Max
	Filter Select = 16 MHz: at 54 MHz	44	33	32	31	dB	Min
	Filter Select = 35 MHz: at 27 MHz	0.7	-0.3/2.7	-0.5/2.8	-0.6/2.9	dB	Min/Max
	Filter Select = 35 MHz: at 74 MHz	28	15	14	13	dB	Min
Mute feed through	Filter Select = Bypass: at 30 MHz	73				dB	
Differential gain	Filter Select = 9 MHz: NTSC/PAL	0.2%/0.35%					
Differential phase	Filter Select = 9 MHz: NTSC/PAL	0.73°/0.86°					
Total harmonic distortion f = 1 MHz, 2 V_{PP}	Filter Select = 9 MHz	–61				dB	
	Filter Select = 16 MHz	–66				dB	
	Filter Select = 35 MHz	–66				dB	
	Filter Select = Bypass	–67				dB	
Signal to noise ratio (unified weighting per CCIR 576-2 recomendation)	Filter Select = 9 MHz, 480i source	84				dB	
	Filter Select = 16 MHz, 480p source	82				dB	
	Filter Select = 35 MHz, 720p source	79				dB	
	Filter Select = Bypass(2), 720p source	67				dB	
Channel-to-Channel Crosstalk	Filter Select = 9 MHz: at 1 MHz	–65				dB	
	Filter Select = 16 MHz: at 1 MHz	–67				dB	
	Filter Select = 35 MHz: at 1 MHz	–69				dB	
	Filter Select = Bypass: at 1 MHz	–70				dB	
MUX Isolation	Filter Select = 9 MHz: at 5.1 MHz	70				dB	
	Filter Select = 16 MHz: at 11 MHz	69				dB	
	Filter Select = 35 MHz: at 27 MHz	71				dB	
	Filter Select = Bypass: at 60 MHz	68				dB	
AC gain – All channels	f = 100 kHz	6	5.7/6.3	5.65/6.35	5.65/6.35	dB	Min/Max
Output impedance	f = 10 MHz	0.7				Ω	

(1) The Min/Max values listed are specified by design only. PCB capacitance affects the filter characteristics, especially the 35-MHz and bypass mode responses.
(2) Bandwidth up to 100-MHz, No Weighting, Tilt Null

ELECTRICAL CHARACTERISTICS, V_{S+} = 5 V (continued)

R_L = 150 Ω to GND, Filter Select = 9 MHz, Input Bias = dc, SAG pin shorted to the output pin (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
DC PERFORMANCE							
Output offset voltage	Bias = dc	30	90	95	95	mV	Max
Average offset voltage drift	Bias = dc				20	µV/°C	
Bias output voltage	Bias = dc + 135 mV, V_I = 0 V	290	235/345	215/360	200/375	mV	Min/Max
	Bias = ac	2.5	2.3/2.7	2.25/2.75	2.25/2.75	V	Min/Max
Sync tip clamp output voltage	Bias = ac STC	300	230/375	215/385	210/390	mV	Min/Max
Input bias current	Bias = dc - implies Ib out of the pin	–0.6	–4	–5	–5	µA	Max
Average bias current drift	Bias = dc				10	nA/°C	
Sync tip clamp bias current	Bias = ac STC, low bias	1.9	0.6/3.3	0.5/3.5	0.4/3.6	µA	Min/Max
	Bias = ac STC, mid bias	6	4.3/8.2	4.1/8.4	4/8.5	µA	Min/Max
	Bias = ac STC, high bias	8.2	6.2/10.8	6/11	5.9/11.1	µA	Min/Max
INPUT CHARACTERISTICS							
Input voltage range	Bias = dc - limited by output	0/2.4	0/2.35	0/2.3	0/2.3	V	Min/Max
Input resistance	Bias = ac bias mode	19				kΩ	
	Bias = dc, dc + 135 mV, ac STC	3				MΩ	
Input capacitance		2				pF	
OUTPUT CHARACTERISTICS							
High output voltage swing	R_L = 150 Ω to midrail	4.8	4.4	4.3	4.3	V	Min
	R_L = 150 Ω to GND	4.65	4.2	4.1	4.1	V	Min
	R_L = 75 Ω to midrail	4.7	4.3	4.2	4.2	V	Min
	R_L = 75 Ω to GND	4.4	4.1	4	4	V	Min
Low output voltage swing	R_L = 150 Ω to midrail	0.2	0.34	0.37	0.37	V	Max
	R_L = 150 Ω to GND	0.1	0.23	0.26	0.27	V	Max
	R_L = 75 Ω to GND	0.35	0.46	0.5	0.5	V	Max
	R_L = 75 Ω to GND	0.1	0.23	0.26	0.27	V	Max
Output current	R_L = 10 Ω to midrail, sourcing	85	60	57	55	mA	Min
	R_L = 10 Ω to midrail, sinking	85	60	57	55	mA	Min
POWER SUPPLY							
Maximum operating voltage		5	5.5	5.5	5.5	V	Max
Minimum operating voltage		5	2.6	2.6	2.6	V	Min
Maximum quiescent current	Per channel V_I = 200 mV	6.6	7.9	8.1	8.2	mA	Max
Minimum quiescent current	Per channel V_I = 200 mV	6.6	5.3	5.1	5	mA	Min
Total quiescent current	All channels ON, V_I = 200 mV(3)	18.9				mA	
Power supply rejection (+PSRR)	V_{S+} = 5.2 V to 4.8 V	66	38	36	36	dB	Min
DISABLE CHARACTERISTICS							
Quiescent current	All 3 channels disabled (4)	0.5				µA	
Turn-on time delay (t_{ON})	Time reaches 50% of final value after I^2C control is completed	5				µs	
Turn-on time delay (t_{OFF})		2				µs	

(3) Due to sharing of internal bias currents, the quiescent current, with all channels operating, is less than the single individual channel quiescent currents added together.

(4) Note that the I^2C circuitry is still active while in Disable mode. The current shown is while there is no activity with the THS7303's I^2C circuitry.

TIMING REQUIREMENTS(1)

V_{S+} = 2.7 V to 5 V

PARAMETER		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	Clock frequency, SCL	0	100	0	400	kHz
$t_{w(H)}$	Pulse duration, SCL high	4		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low	4.7		1.3		µs
t_r	Rise time, SCL and SDA		1000		300	ns
t_f	Fall time, SCL and SDA		300		300	ns
$t_{su(1)}$	Setup time, SDA to SCL	250		100		ns
$t_{h(1)}$	Hold time, SCL to SDA	0		0		ns
$t_{(buf)}$	Bus free time between stop and start conditions	4.7		1.3		µs
$t_{su(2)}$	Setup time, SCL to start condition	4.7		0.6		µs
$t_{h(2)}$	Hold time, start condition to SCL	4		0.6		µs
$t_{su(3)}$	Setup time, SCL to stop condition	4		0.6		µs
C_b	Capacitive load for each bus line		400		400	pF

(1) The THS7303 I^2C address = 01011(A1)(A0)(R/W). See the application information section for more information.

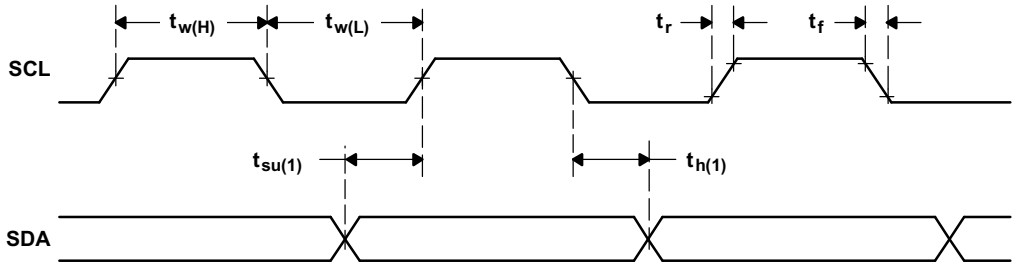


Figure 2. SCL and SDA Timing

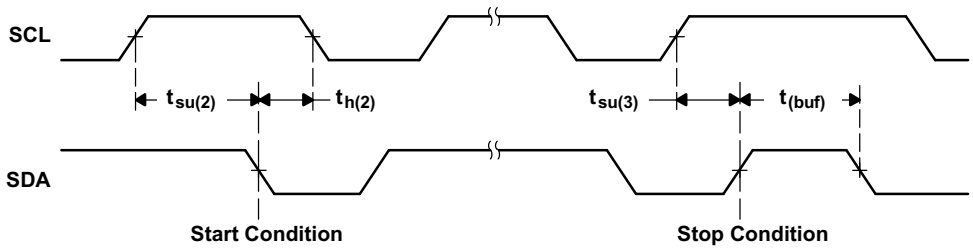
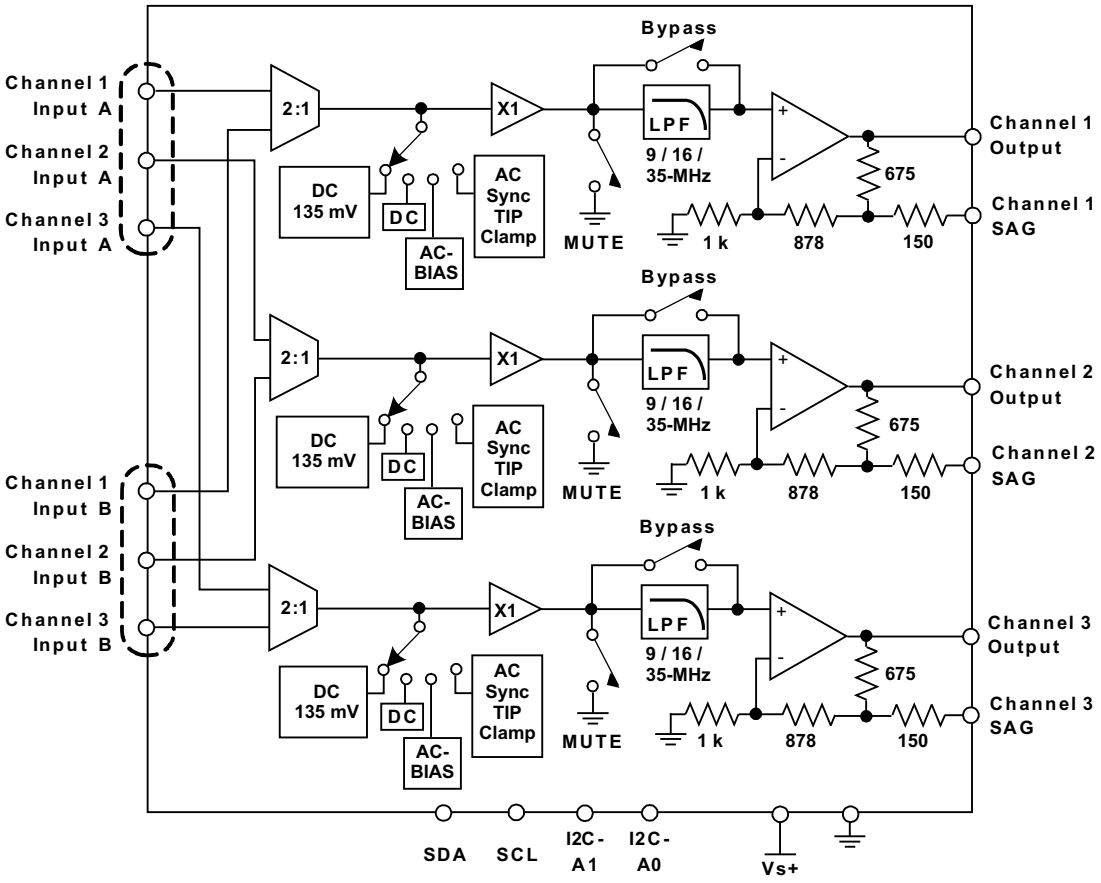


Figure 3. Start and Stop Conditions

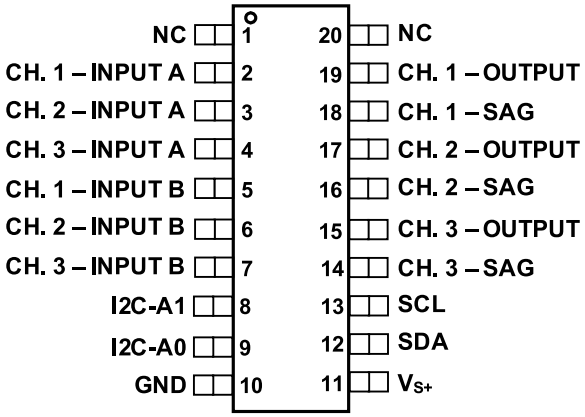
FUNCTIONAL DIAGRAM



NOTE: The I^2C Address of the THS7303 is 01011(A1)(A0)(R/W)

PIN CONFIGURATION

THS7303PW
TSSOP (20-Pin)
(Top View)



A. NC indicates there is no internal connection to these pins.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
N/C	1, 20	No Internal Connection
CH. 1 – INPUT A	2	Video Input Channel 1. Input A
CH. 2 – INPUT A	3	Video Input Channel 2. Input A
CH. 3 – INPUT A	4	Video Input Channel 3. Input A
CH. 1 – INPUT B	5	Video Input Channel 1. Input B
CH. 2 – INPUT B	6	Video Input Channel 2. Input B
CH. 3 – INPUT B	7	Video Input Channel 3. Input B
I2C-A1	8	I^2C Slave Address Control Bit A.1 Connect to Vs+ for a logic 1 preset value or GND for a logic 0 preset value.
I2C-A0	9	I^2C Slave Address Control Bit A0. Connect to Vs+ for a logic 1 preset value or GND for a logic 0 preset value.
GND	10	Ground reference pin for all internal circuitry
Vs+	11	Positive Power Supply Input Pin. Connect to 2.7 V to 5 V
SDA	12	Serial data line of the I^2C bus. Pull-up resistor should have a minimum value = 2-kΩ and a maximum value = 19-kΩ. Pull up to Vs+
SCL	13	I^2C bus Clock Line. Pull-up resistor should have a minimum value = 2-kΩ and a maximum value = 19-kΩ. Pull up to Vs+
CH. 3 - SAG	14	Video output channel 3 SAG Correction Pin. If SAG is not used, connect directly to CH. 3 – OUTPUT pin.
CH. 3 – OUTPUT	15	Video output channel 3 from either CH. 3 – INPUT A or CH. 3 – INPUT B
CH. 2 - SAG	16	Video output channel 2 SAG correction pin. If SAG is not used, connect directly to CH. 2 – OUTPUT pin.
CH. 2 – OUTPUT	17	Video output channel 2 from either CH. 2 – INPUT A or CH. 2 – INPUT B
CH. 1 - SAG	18	Video output channel 1 SAG correction pin. If SAG is not used, connect directly to CH. 1 – OUTPUT pin.
CH. 1 – OUTPUT	19	Video output channel 1 from either CH. 1 – INPUT A or CH. 1 – INPUT B

TYPICAL CHARACTERISTICS

SMALL-SIGNAL FREQUENCY RESPONSE

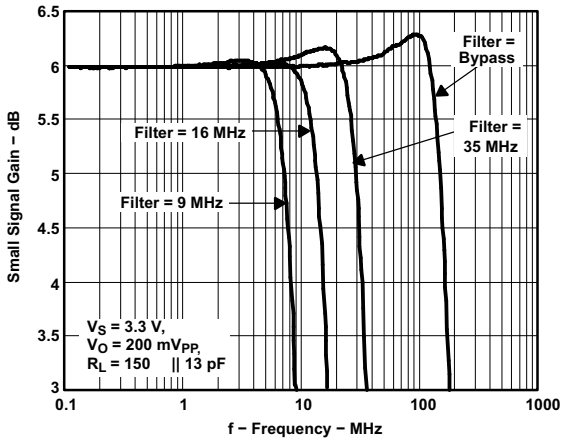


Figure 4.

SMALL-SIGNAL FREQUENCY RESPONSE

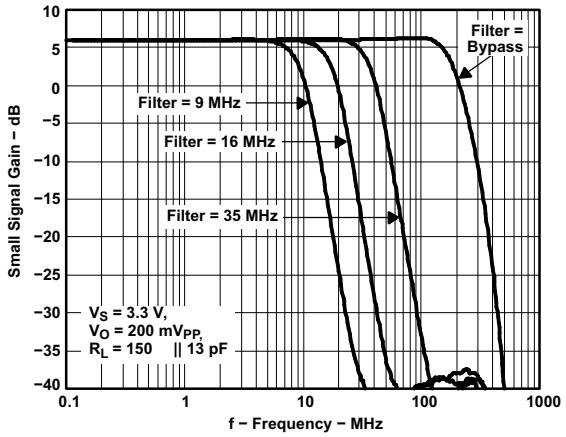


Figure 5.

GROUP DELAY vs FREQUENCY

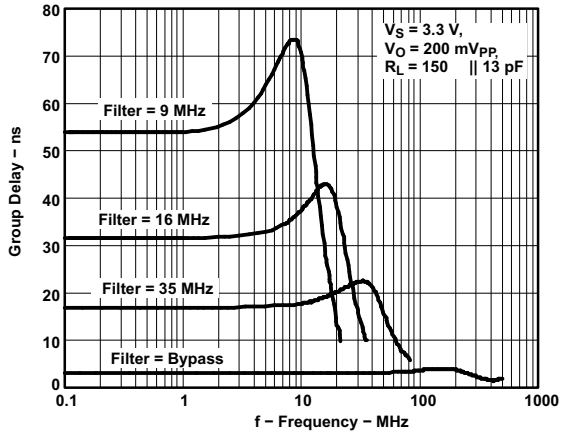


Figure 6.

PHASE RESPONSE vs FREQUENCY

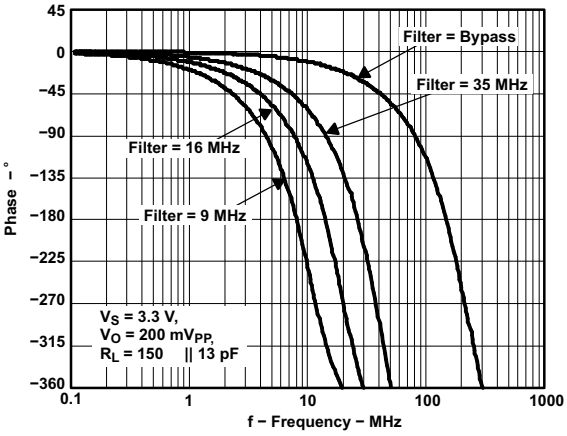


Figure 7.

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

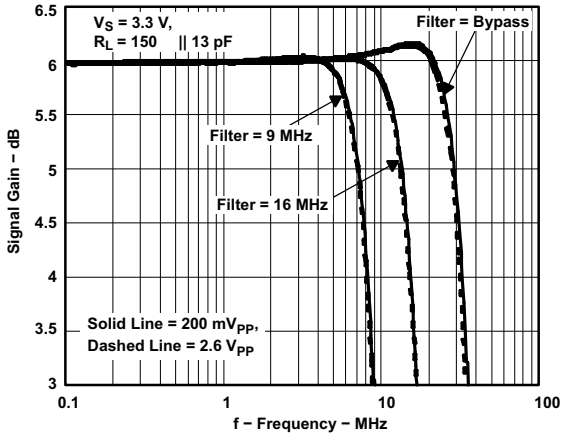


Figure 8.

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

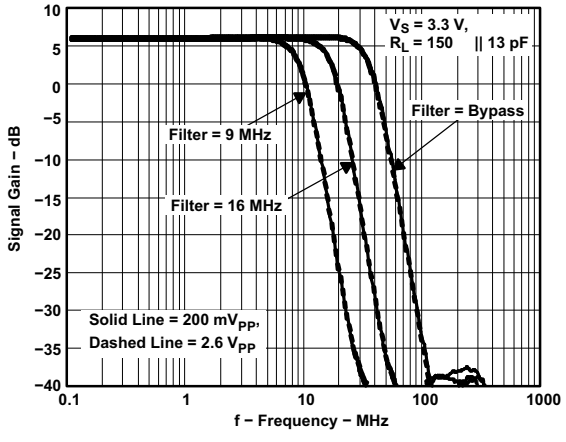


Figure 9.

TYPICAL CHARACTERISTICS (continued)

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

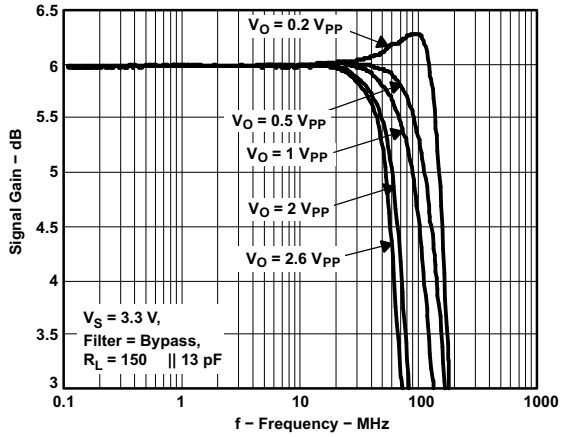


Figure 10.

OUTPUT IMPEDANCE vs FREQUENCY

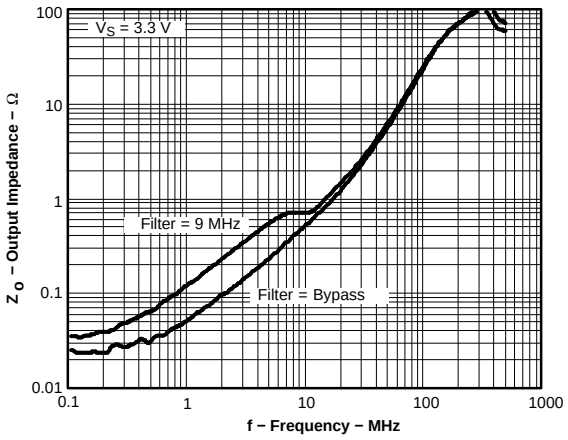


Figure 11.

3.3 V DIFFERENTIAL GAIN

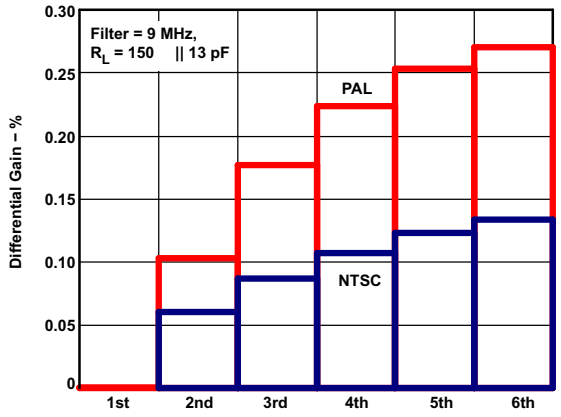


Figure 12.

3.3 V DIFFERENTIAL PHASE

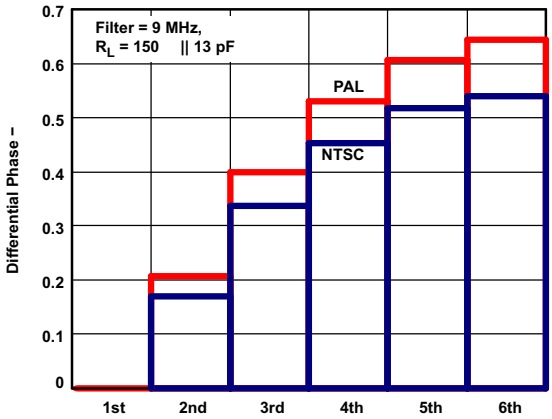


Figure 13.

HD2 vs FREQUENCY

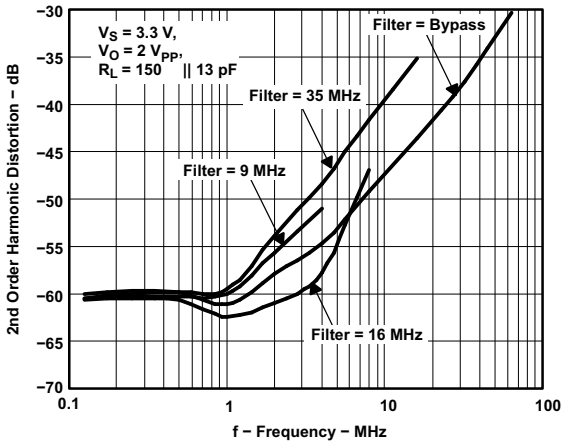


Figure 14.

HD3 vs FREQUENCY

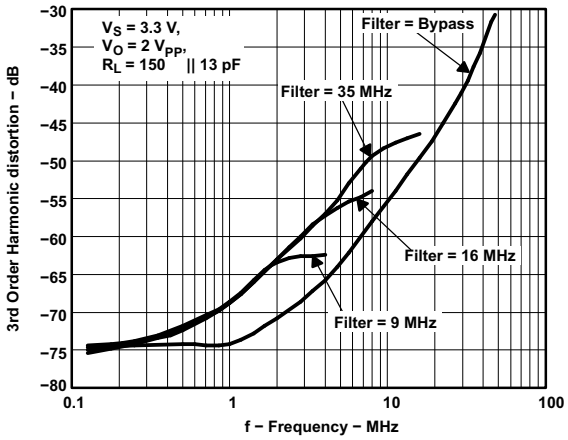


Figure 15.

TYPICAL CHARACTERISTICS (continued)

HD2 vs OUTPUT VOLTAGE

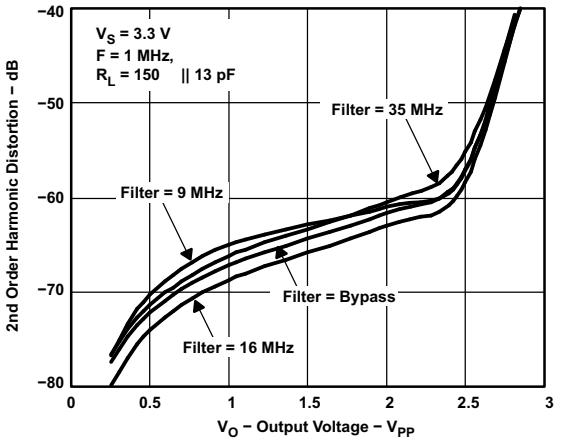


Figure 16.

HD3 vs OUTPUT VOLTAGE

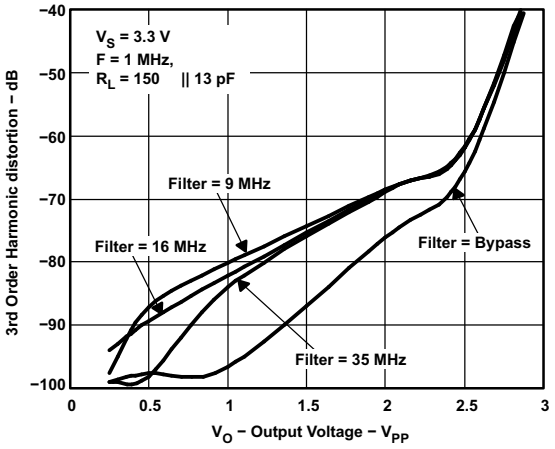


Figure 17.

SMALL SIGNAL FREQUENCY RESPONSE WITH CAPACITIVE LOADS

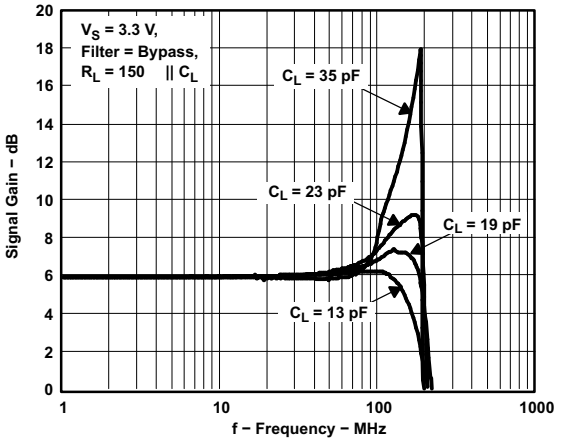


Figure 18.

SMALL SIGNAL FREQUENCY RESPONSE WITH 19 pF CAPACITIVE LOAD

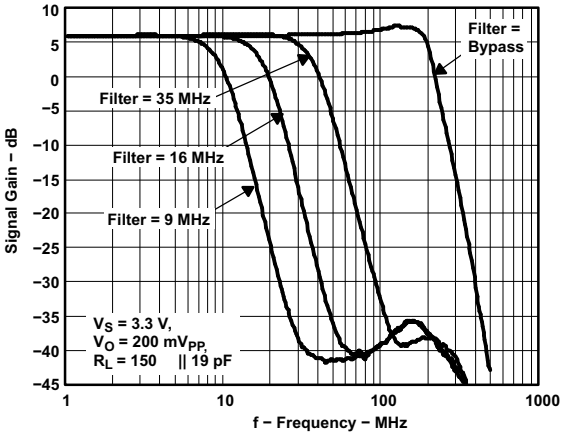


Figure 19.

SMALL SIGNAL FREQUENCY RESPONSE WITH 23 pF CAPACITIVE LOAD

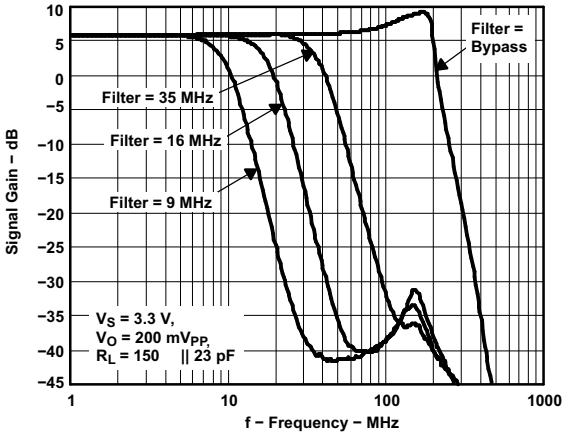


Figure 20.

SMALL SIGNAL FREQUENCY RESPONSE WITH 35 pF CAPACITIVE LOAD

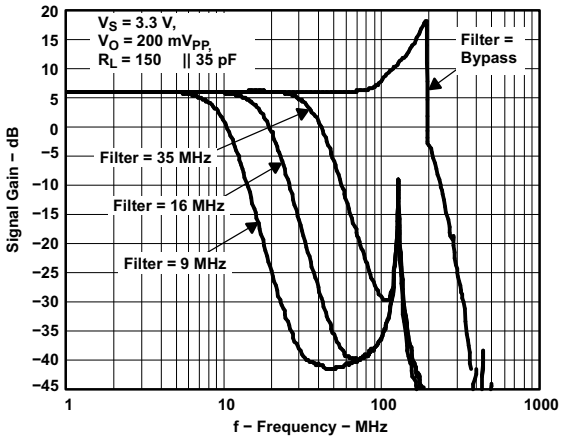


Figure 21.

TYPICAL CHARACTERISTICS (continued)

SMALL SIGNAL PULSE RESPONSE

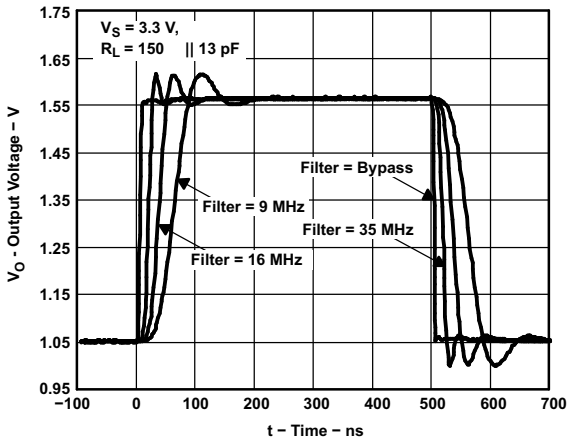


Figure 22.

LARGE SIGNAL PULSE RESPONSE

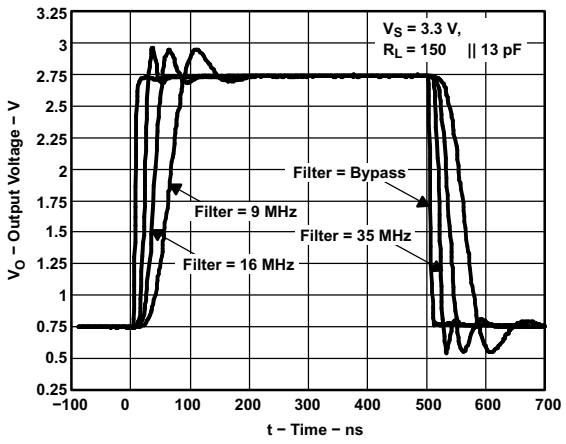


Figure 23.

NTSC - 2T RESPONSE

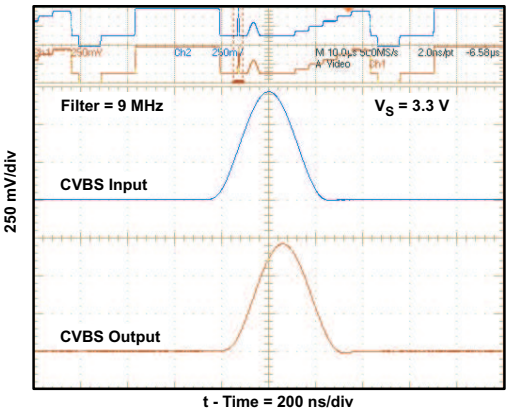


Figure 24.

PAL - 12.5T RESPONSE

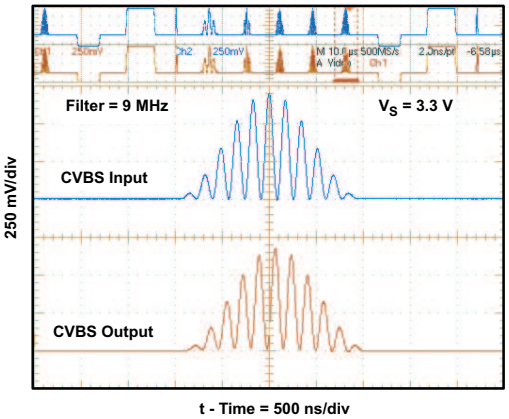


Figure 25.

576p - 2T PULSE RESPONSE

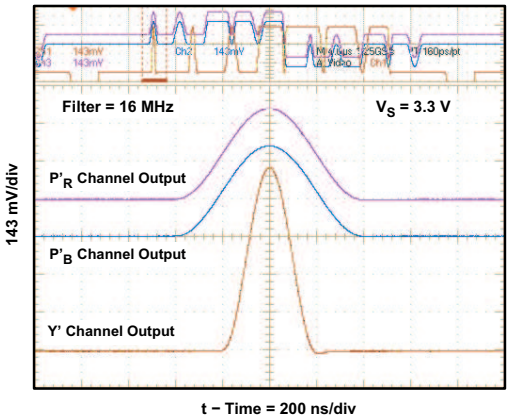


Figure 26.

720p - 2T PULSE RESPONSE

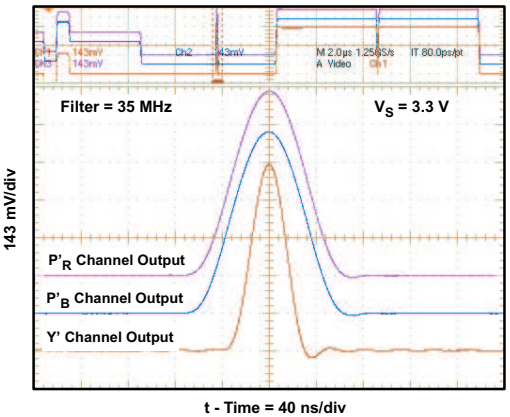


Figure 27.

TYPICAL CHARACTERISTICS (continued)

SLEW RATE vs OUTPUT VOLTAGE

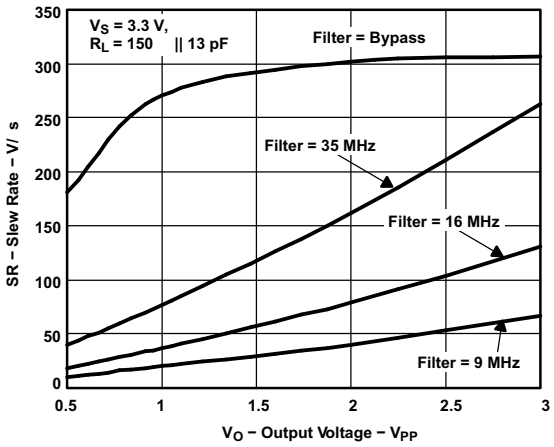


Figure 28.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

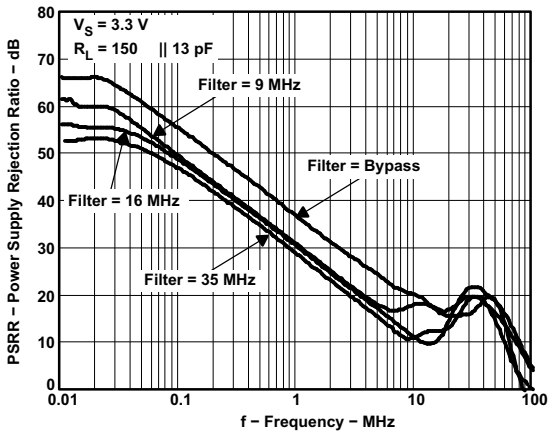


Figure 29.

MUX FEED THROUGH vs FREQUENCY

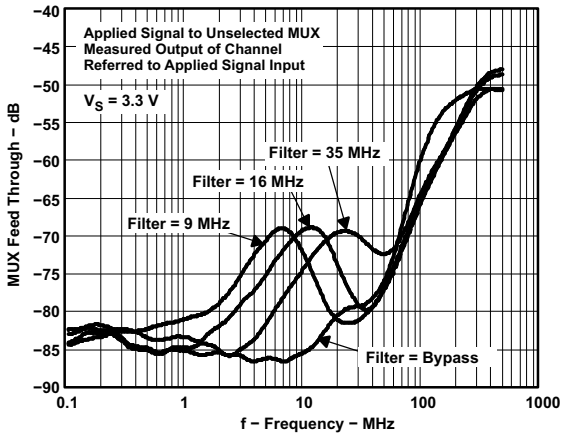


Figure 30.

MUTE FEED THROUGH vs FREQUENCY

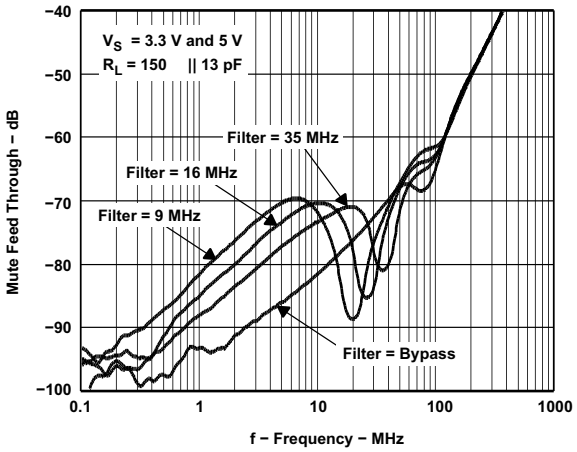


Figure 31.

CROSSTALK vs FREQUENCY

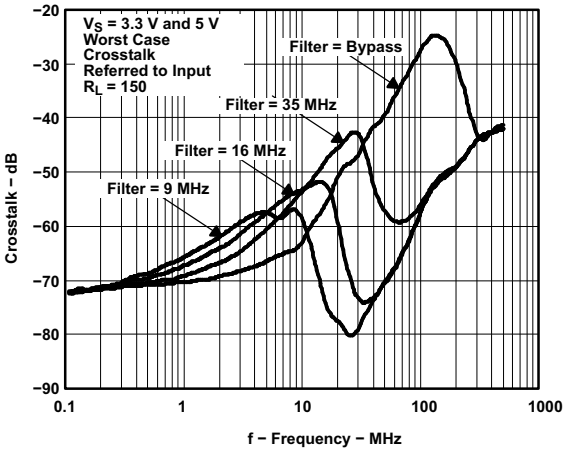


Figure 32.

TOTAL QUIESCENT CURRENT vs SUPPLY VOLTAGE

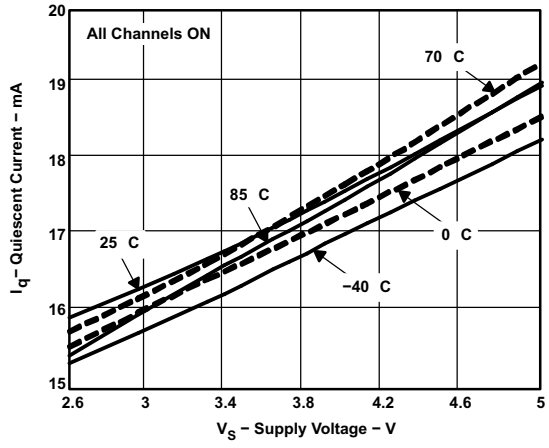


Figure 33.

TYPICAL CHARACTERISTICS (continued)

INPUT BIAS CURRENT vs TEMPERATURE

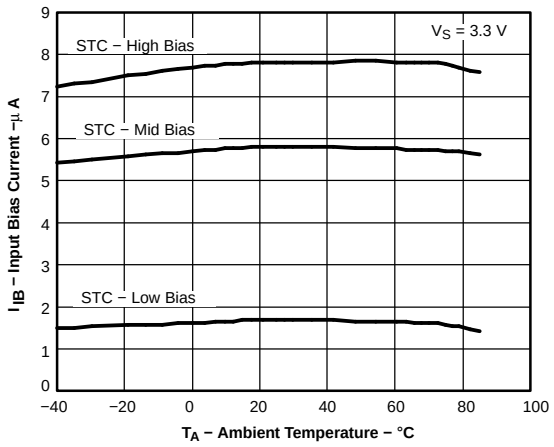


Figure 34.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

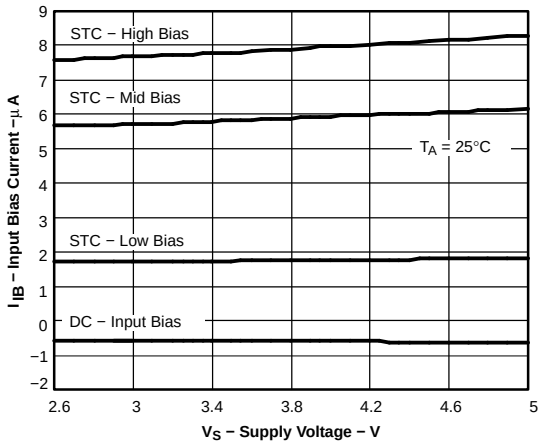


Figure 35.

SMALL SIGNAL FREQUENCY RESPONSE

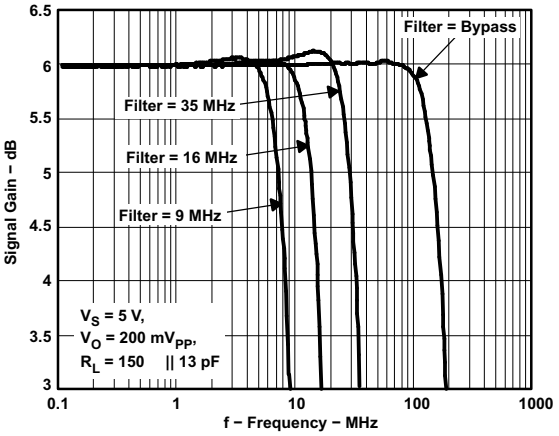


Figure 36.

SMALL SIGNAL FREQUENCY RESPONSE

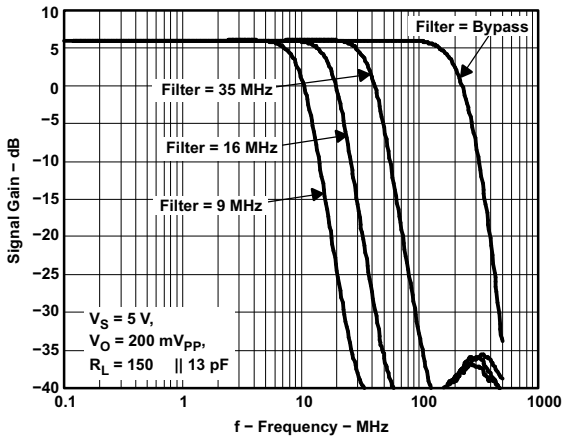


Figure 37.

GROUP DELAY vs FREQUENCY

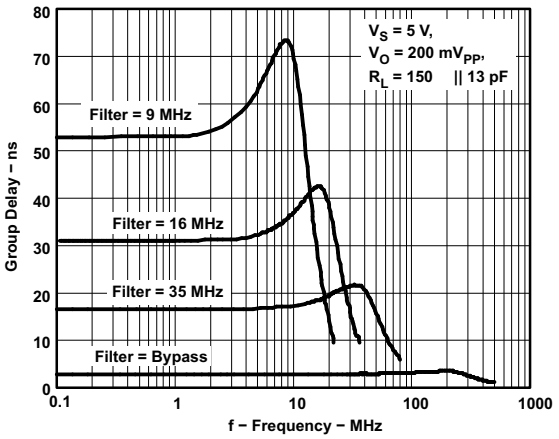


Figure 38.

PHASE vs FREQUENCY

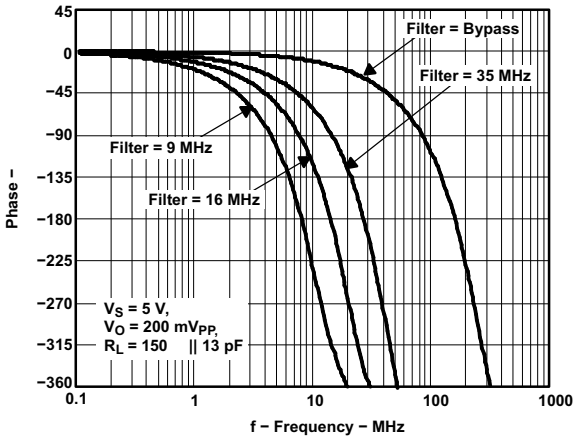


Figure 39.

TYPICAL CHARACTERISTICS (continued)

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

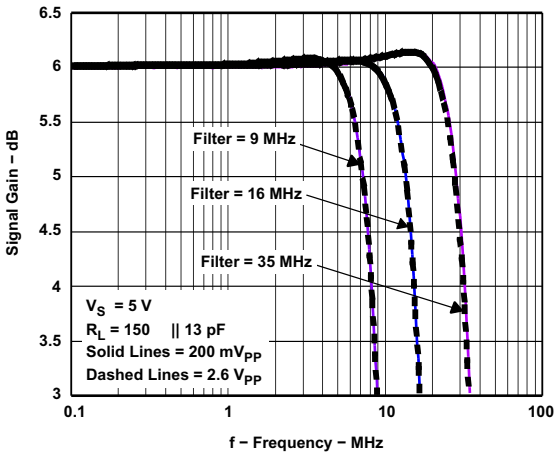


Figure 40.

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

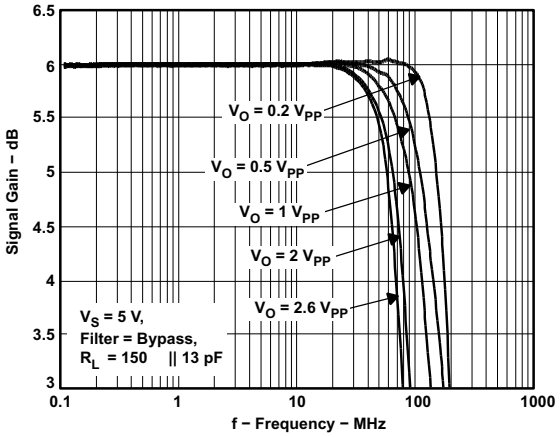


Figure 41.

5 V DIFFERENTIAL GAIN

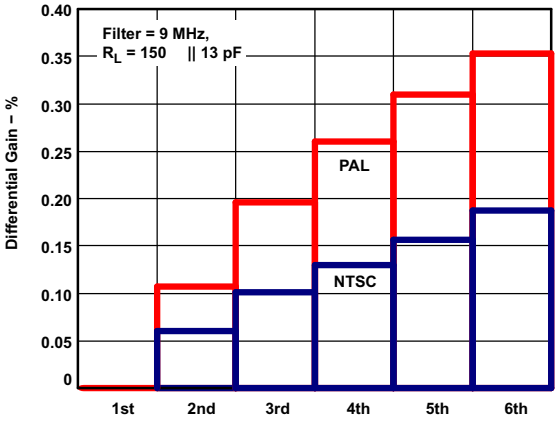


Figure 42.

5 V DIFFERENTIAL PHASE

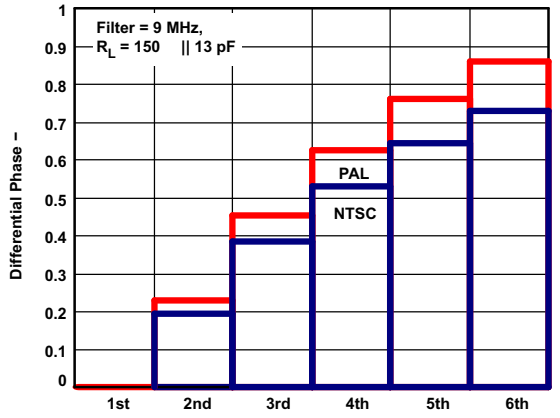


Figure 43.

HD2 vs FREQUENCY

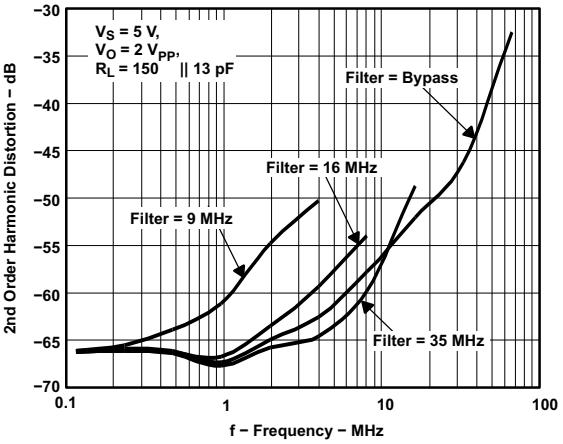


Figure 44.

HD3 vs FREQUENCY

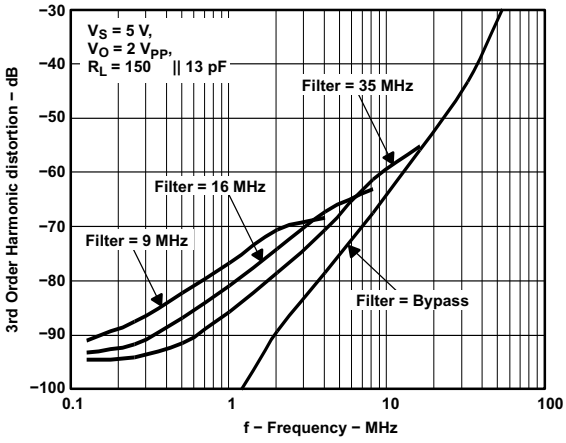


Figure 45.

TYPICAL CHARACTERISTICS (continued)

HD2 vs OUTPUT VOLTAGE

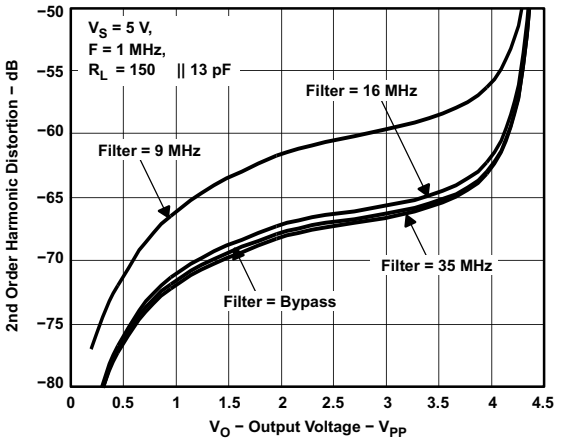


Figure 46.

HD3 vs OUTPUT VOLTAGE

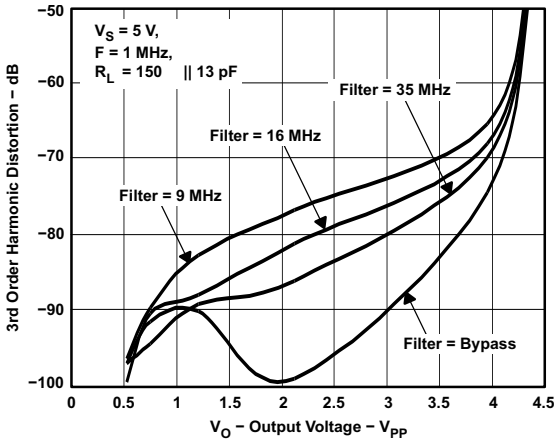


Figure 47.

SMALL SIGNAL FREQUENCY RESPONSE CAPACITIVE LOAD

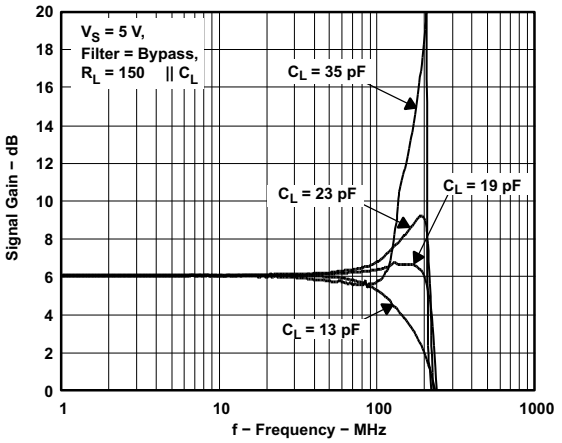


Figure 48.

SMALL SIGNAL FREQUENCY RESPONSE WITH 19 pF CAPACITIVE LOAD

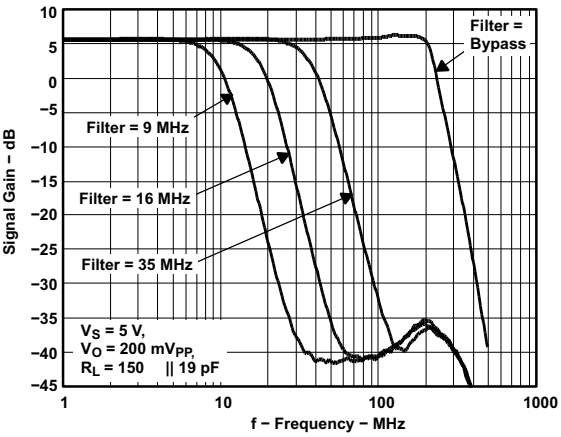


Figure 49.

SMALL SIGNAL FREQUENCY RESPONSE WITH 23 pF CAPACITIVE LOAD

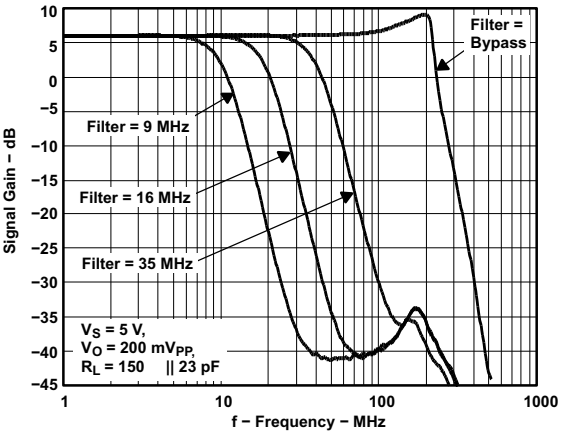


Figure 50.

SMALL SIGNAL FREQUENCY RESPONSE WITH 35 pF CAPACITIVE LOAD

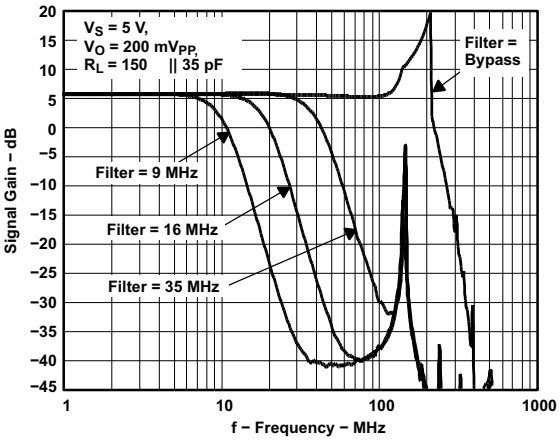


Figure 51.

TYPICAL CHARACTERISTICS (continued)

SMALL SIGNAL PULSE RESPONSE

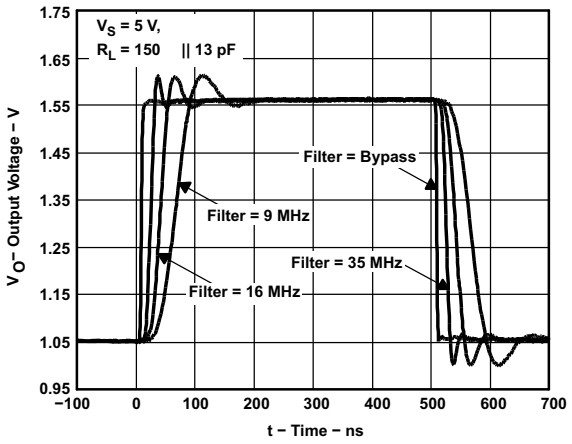


Figure 52.

LARGE SIGNAL PULSE RESPONSE

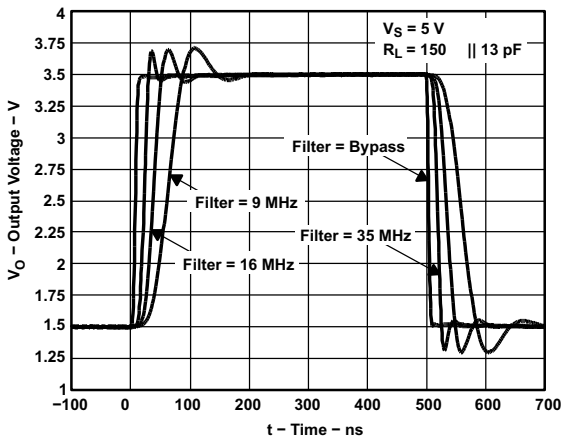


Figure 53.

SLEW RATE vs OUTPUT VOLTAGE

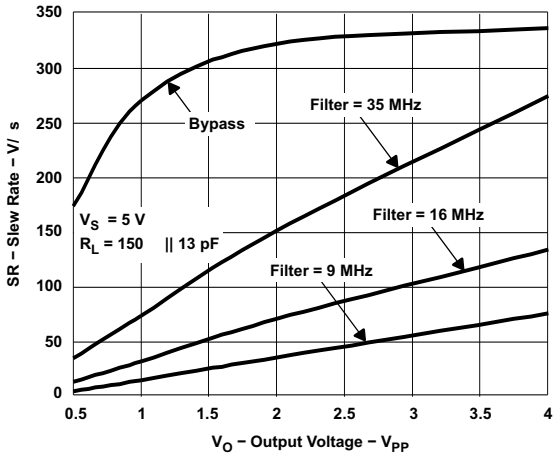


Figure 54.

OUTPUT IMPEDANCE vs FREQUENCY

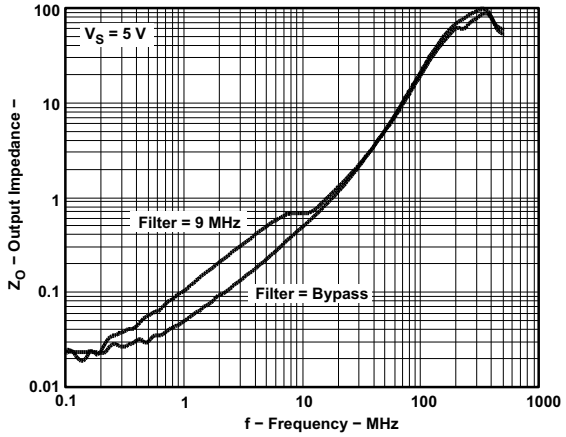


Figure 55.

MUX FEED-THROUGH vs FREQUENCY

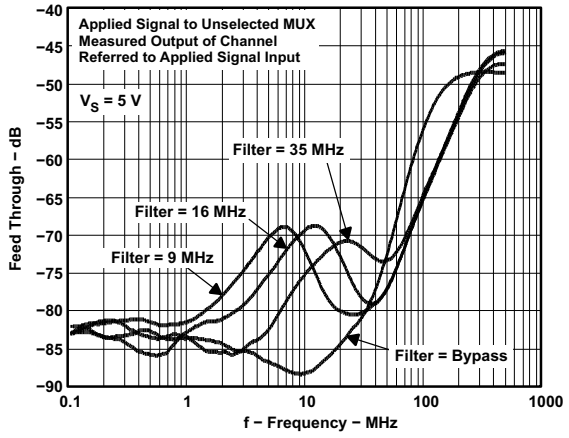


Figure 56.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

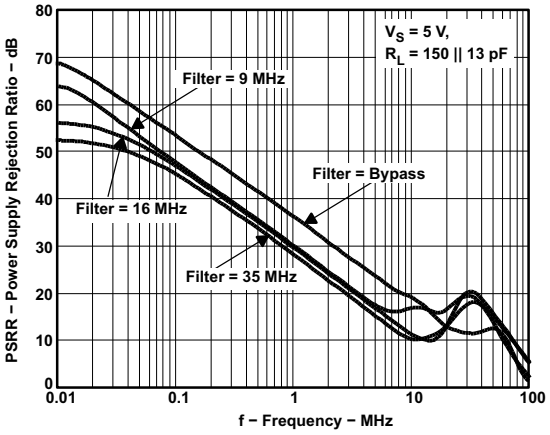


Figure 57.

APPLICATION INFORMATION

The THS7303 is targeted for video output buffer applications. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the THS7303. Built on the complimentary silicon germanium (SiGe) BiCom-3 process, the THS7303 incorporates many features not typically found in integrated video parts while consuming low power. Each channel configuration is completely independent of the other channels. This allows for configurations for each channel to be dictated by the end user and not the device. This results in a highly flexible system for most video systems. The THS7303 contains the following features:

- I^2C Interface for easy interfacing to the system.
- Single-supply 2.7-V to 5-V operation with low total quiescent current of 16.6 mA with 3.3-V supply and 18.9 mA with 5-V supply.
- 2:1 input MUX.
- Input configuration accepting dc, dc + 135 mV shift, ac bias, or ac sync-tip clamp selection.
- Selectable 5^{th} order, low-pass filter for DAC reconstruction or ADC image rejection :
  - 9-MHz for SDTV NTSC and 480i, PAL/SECAM and 576i, S-Video, and G'B'R' (R'G'B') signals.
  - 16-MHz for EDTV 480p and 576p $Y'P'_BP'_R$ signals, G'B'R', and VGA signals.
  - 35-MHz for HDTV 720p and 1080i $Y'P'_BP'_R$ signals, G'B'R', and SVGA/XGA signals.
  - Bypass mode for passing HDTV 1080p $Y'P'_BP'_R$, G'B'R', and SXGA/UXGA signals.
- Internal fixed gain of 2 V/V (6 dB) buffer that can drive 2 video lines with dc coupling, traditional ac coupling, or SAG corrected ac coupling.
- Disable mode which reduces quiescent current to as low as 0.1-μA or a mute function that keeps the THS7303 powered on, but does not allow a signal to pass through.
- Signal flow-through configuration using a 20-pin TSSOP package that complies with the latest lead-free (RoHS compatible) and green manufacturing requirements.

OPERATING VOLTAGE

The THS7303 is designed to operate from 2.7 V to 5 V over a -40°C to 85°C temperature range. The impact on performance over the entire temperature range is negligible due to the implementation of thin film resistors and low-temperature coefficient capacitors.

The power supply pins should have a 0.1-μF to 0.01-μF capacitor placed as close as possible to these pins. Failure to do so may result in the THS7303 outputs ringing or oscillating. Additionally, a large capacitor, such as 22 μF to 100 μF, should be placed on the power supply line to minimize issues with 50/60 Hz line frequencies.

INPUT VOLTAGE

The THS7303 input range allows for an input signal range from ground to (V_{S+}– 1.4 V). But, due to the internal fixed gain of 2 V/V (6 dB), the output is the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from GND to 3.6 V. But due to the gain, the linear output range limits the allowable linear input range to be from GND to a maximum of 2.5 V.

INPUT OVERVOLTAGE PROTECTION

The THS7303 is built using a high-speed complementary bipolar and CMOS process. The internal junction breakdown voltages are low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 58.

APPLICATION INFORMATION (continued)

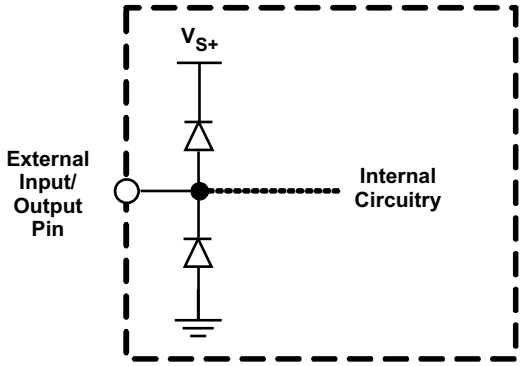


Figure 58. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies. The protection diodes can typically support 30-mA of continuous current when overdriven.

TYPICAL CONFIGURATION and VIDEO TERMINOLOGY

A typical application circuit using the THS7303 as a video buffer is shown in Figure 59. It shows a DAC (or encoder such as the THS8200) driving the three input channels of the THS7303. Although the high-definition video (HD) or enhanced-definition (ED) $Y'P'_BP'_R$ (sometimes Y'U'V' is used or it is incorrectly labeled $Y'C'_BC'_R$) channels are shown, these channels can easily be S-Video Y'C' channels and the composite video baseband signal (CVBS) of a standard definition video (SD) system. These signals can also be G'B'R' (R'G'B') signals or other variations. Note that for computer signals the sync should be embedded within the signal for a system with only 3-outputs. This is sometimes labeled as R'G'sB' (sync on green) or R'sG'sB's (sync on all signals).

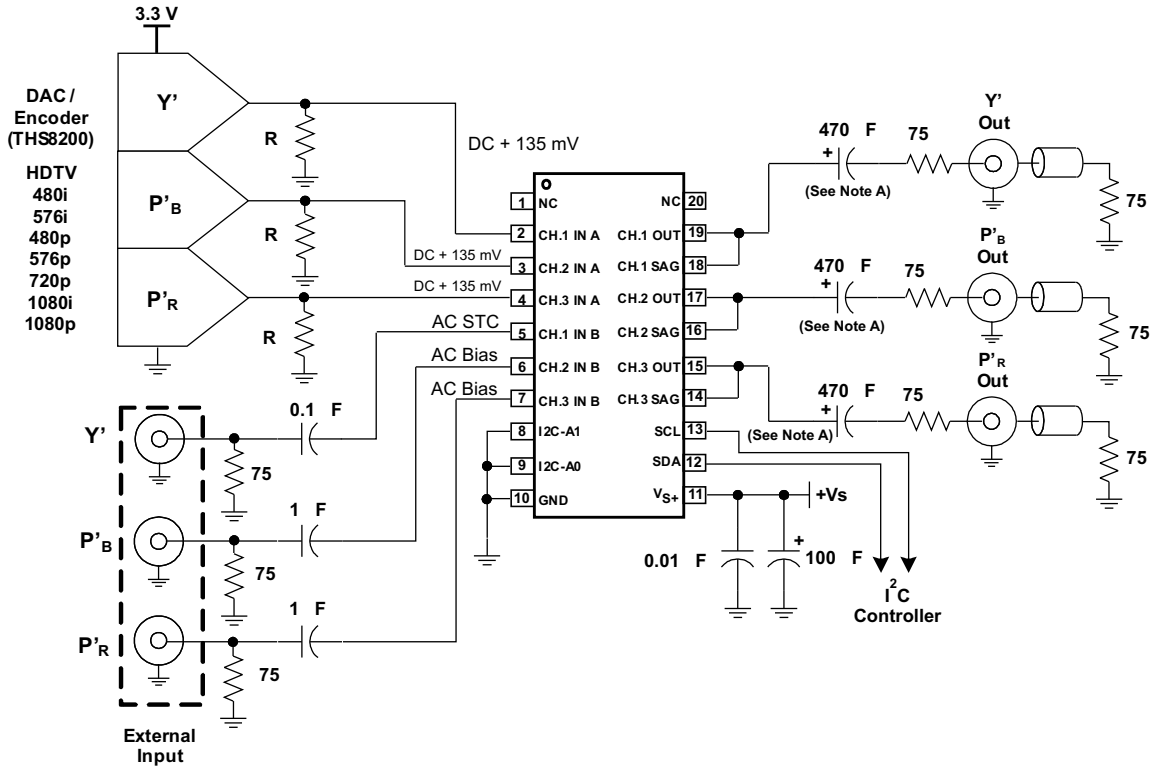
The second set of inputs (B-Channels) shown are being driven from an external input typically used as a pass-through function. These are either HD, ED, or SD video signals. The flexibility of the THS7303 allows for almost any input signal to be driven into the THS7303 regardless of the other set of inputs. Control of the I^2C configures each channel of the THS7303 independently of the other channels. For example, the THS7303 can be configured to have Channel 1 Input connected to input A with 35-MHz LPF while Channels 2 and 3 are connected to input B with 16-MHz LPF. See the various sections explaining the I^2C interface later in this data sheet for more information.

Note that the Y' term is used for the luma channels throughout this document rather than the more common luminance (Y) term. The reason is to account for the definition of luminance as stipulated by the CIE - International Commission on Illumination. Video departs from true luminance since a nonlinear term, gamma, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus luminance (Y) is not maintained providing a difference in terminology.

This rationale is also used for the chroma (C') term. Chroma is derived from the non-linear R'G'B' terms and thus it is nonlinear. Chominance (C) is derived from linear RGB giving the difference between chroma (C') and chrominance (C). The color difference signals (P'_B / P'_R / U' / V') are also referenced this way to denote the nonlinear (gamma corrected) signals.

R'G'B' (commonly mislabeled RGB) is also called G'B'R' (again commonly mislabeled as GBR) in professional video systems. The SMPTE component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This is consistent with the $Y'P'_BP'_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Since the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel respectfully. Thus hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems sync is embeded on all three channels, but may not always be the case in all systems.

APPLICATION INFORMATION (continued)



A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-µF capacitor in parallel with these large capacitors.

Figure 59. Typical Y'P'$_B$P'$_R$ Inputs From DC-Coupled Encoder/DAC and AC-Coupled External Inputs With AC-Coupled Line Driving

INPUT MODES OF OPERATION – DC

The inputs to the THS7303 allows for both ac coupled and dc coupled inputs. Many DAC's or video encoders can be dc connected to the THS7303. But, one of the drawbacks to dc coupling is when 0 V is applied to the input of the THS7303. Although the input of the THS7303 allows for a 0-V input signal, the output swing of the THS7303 cannot yield a 0-V signal. This applies to any traditional single-supply amplifier due to the limitations of the output transistors. Both CMOS and bipolar transistors cannot go to 0 V while sinking a significant amount of current. This trait of a transistor is also the same reason why the highest output voltage is always less than the power supply voltage when sourcing a significant amount of current.

The internal gain is fixed at 6 dB (2 V/V) regardless of the configuration of the THS7303, and dictates what the allowable linear input voltage range is without clipping concerns. For example, if the power supply is set to 3 V, the maximum output is about 2.9 V. Thus, to avoid clipping, the allowable input is 2.9 V / 2 = 1.45 V. This is true for up to the maximum recommended 5-V power supply that allows about a 4.9 V / 2 = 2.45 V input range while avoiding clipping on the output.

The input impedance of the THS7303 in this mode of operation is >1 MΩ. This is due to the input buffer being configured as a unity gain amplifier as shown in Figure 60.

APPLICATION INFORMATION (continued)

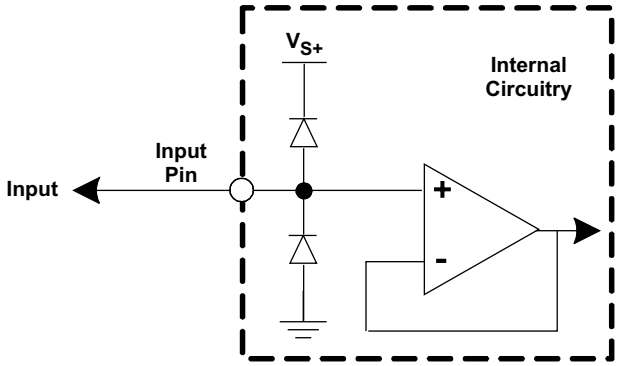


Figure 60. Equivalent DC Input Mode Circuit

The input stage of the THS7303 is designed with PNP bipolar transistors. There is a finite amount of bias current flowing *out* of the THS7303 input pin. This bias current, typically about 0.6 μA, must have a path to flow or else the input stage voltage increases. For example, if there is a 1-MΩ resistance to ground on the input node, the resulting voltage appearing at the input node is 0.6 μA x 1 MΩ = 0.6 V. Therefore, it should be noted that if a channel is powered on and has no input termination, the input bias current causes the input stage to *float* high until saturation of the input stage exists - about 1.4 V from the power supply. Typically, this is not a concern as most terminations result in an equivalent source impedance of 75-Ω to 300-Ω.

INPUT MODES OF OPERATION – DC + 135 mV SHIFT

Clipping occurs with a 0-V applied input signal when the input mode is set to dc. The clipping can reduce the sync amplitudes (both horizontal and vertical sync amplitudes) on the video signal. A problem occurs if the receiver of this video signal uses an AGC loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much – resulting in too much luma and/or chroma amplitude gain correction. This may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits use the chroma burst amplitude for amplitude control, and a reduction in the sync signals does not alter the proper gain setting. But, it is good engineering design practice to ensure saturation/clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations on the signals.

To eliminate saturation / clipping problems, the THS7303 has a dc + 135 mV shift input mode. This mode takes the input voltage and adds an internal +135 mV shift to the signal. Since the THS7303 also has a gain of 6 dB (2 V/V), the resulting output with a 0-V applied input signal is about 270 mV. The THS7303 rail-to-rail output stage can create this level while connected to a typical video load. This ensures that no saturation / clipping of the sync signals occurs. This is a constant shift regardless of the input signal. For example, if a 1-V input is applied, the output is at 2.27 V.

As with the dc-input mode, the input impedance of the THS7303 is > 1 MΩ. Additionally, the same input bias current of about 0.6 μA appears at the input. Following the same precautions as stipulated with the dc-input mode of operation minimizes any potential issues. Figure 61 shows the equivalent input circuit while in the dc + 135 mV shift mode of operation. Note that the internal voltage shift does not appear at the input pin, only the output pin.

APPLICATION INFORMATION (continued)

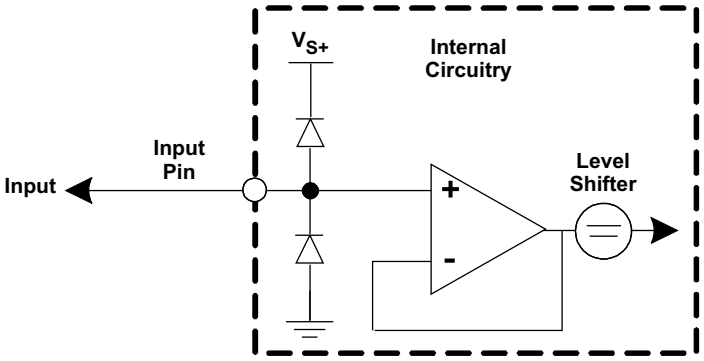


Figure 61. Equivalent DC + 135 mV Input Mode Circuit

INPUT MODES OF OPERATION – AC BIAS

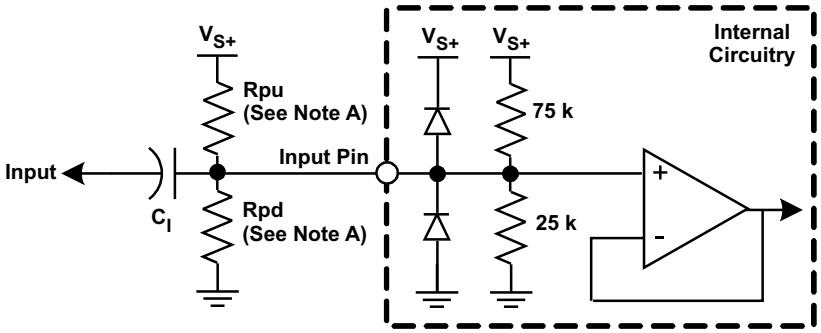
Other applications require an ac-coupled input. The ac coupling ensures that a source dc-input level does not alter, or clip, the resulting output video signal. The first ac coupling mode is the AC Bias mode where a simple internal dc bias voltage is applied to the input signal on the THS7303 side of the external 1-µF coupling capacitor.

The applied dc bias voltage is set internally by a simple resistor divider circuit as shown in Figure 62. The dc bias voltage is set to V_{S+}÷ 4. With a 3.3-V power supply, the input bias voltage is nominally 0.825 V, and with 5-V supply, the input bias voltage is nominally 1.25 V. The input impedance with this mode is approximately 19-kΩ. With a 1-µF input capacitor, it sets a high-pass corner frequency of about 9-Hz. If a lower frequency is desired, increasing the capacitor decreases the corner frequency proportionally. For example, using a 4.7-µF capacitor results in a 1.8-Hz high pass corner frequency, and results in lower droop (tilt). Using any capacitor value is acceptable for this mode of operation.

It is sometimes desirable to adjust the bias voltage to another level other than the one dictated by the internal resistors. There are two ways this is accomplished:

1. The first is to add an external resistor between the input pin and either the +Vs or GND. This creates a new bias voltage equal to +Vs × [25 k / {25 k + (75 k || Rpu)}] for raising the bias voltage, or +Vs × [(25 k || Rpd) / {(25 k || Rpd) + 75 k}] for reducing the bias voltage.
2. The second method to set the AC-Bias voltage is to use the Rpu and Rpd external resistors, but place the THS7303 in dc input bias mode. Since the dc mode is very high impedance, the resulting bias voltage is equal to +Vs × (Rpd / {Rpd + Rpu}).

This mode of operation is recommended for use with chroma (C'), P'_B, P'_R, U', V', and other nonsync signals.



NOTE: Use external pull-up and/or pull-down resistors if changing the AC-bias input voltage is desired.

Figure 62. Equivalent AC Bias Input Mode Circuit

APPLICATION INFORMATION (continued)

INPUT MODES OF OPERATION – AC SYNC TIP CLAMP

The last input mode of operation is the ac with sync-tip-clamp (STC) which also requires a capacitor in series with the input. Note that while the term sync-tip-clamp is used throughout this document, the THS7303 is better termed as a dc restoration circuit based on the way this function is performed. This circuit is an active clamp circuit and not a passive diode clamp function. This function should be used when ac coupling is desired with signals that have sync signals embedded such as CVBS, Y', and G' signals.

The input to the THS7303 has an internal control loop which sets the lowest input applied voltage to clamp at approximately 135 mV. Like the dc + 135 mV input shift, the resulting output voltage low level is about 270 mV. If the input signal tries to go below the 135-mV level, the internal control loop of the THS7303 sources up to 2 mA of current to increase the input voltage level on the THS7303 input side of the coupling capacitor. As soon as the voltage goes above the 135-mV level, the loop stops sourcing current.

One of the concerns about the sync-tip-clamp level is how the clamp reacts to a sync edge that has overshoot – common in VCR signals or reflections found in poor PCB layouts. Ideally the STC should not react to the overshoot voltage of the input signal. Otherwise, this could result in clipping on the rest of the video signal because there may be too much increase in the bias voltage.

To help minimize this input signal overshoot problem, the patent-pending internal STC control loop in the THS7303 has an I^2C selectable low-pass filter as shown in Figure 63. This filter can be selected to be about 500 kHz, 2.5 MHz, or 5 MHz. The 500-kHz filter is useful when the THS7303's 5^{th}-order low pass filter is selected for 9-MHz operation. The effect of this filter is to slow down the response of the control loop so as not to clamp on the input overshoot voltage, but rather the flat portion of the sync signal when the ringing should be settled out. The 2.5-MHz filter is best suited for use in conjunction with the 16-MHz signal LPF to account for the faster sync times associated with the higher rate video signals. For HDTV signals, the 5-MHz STC filter should be selected to allow for the faster sync rates to properly set the clamp level. Any STC filter can be selected regardless of the signal or system filter.

As a result of this selectable delay, the sync has an apparent voltage shift occurring between 15 ns and 2 µs after the sync falling edge – depending on the STC LPF. The amount of shift is dependant upon the amount of droop in the signal as dictated by the input capacitor and the STC input bias current selection. Because the sync is primarily for timing purposes with syncing occurring on the edge of the sync signal, this shift is transparent in most systems. Note that if the source signal is known to be good, selecting the 5-MHz STC LPF is recommended for all sources

While this feature may not fully eliminate overshoot issues on the input signal in case of really bad overshoot and/or ringing, the STC system should help minimize improper clamping levels. As an additional method to help minimize this issue, an external capacitor (example: 10 pF to 47 pF) to ground in parallel with the external termination resistors can help filter overshoot problems.

It should be noted that this STC system is dynamic and does not rely upon timing in any way. It only depends on the voltage appearing at the input pin at any given point in time. The STC filtering helps minimize level shift problems associated with switching noises or short spikes on the signal line. This helps ensure a robust STC system.

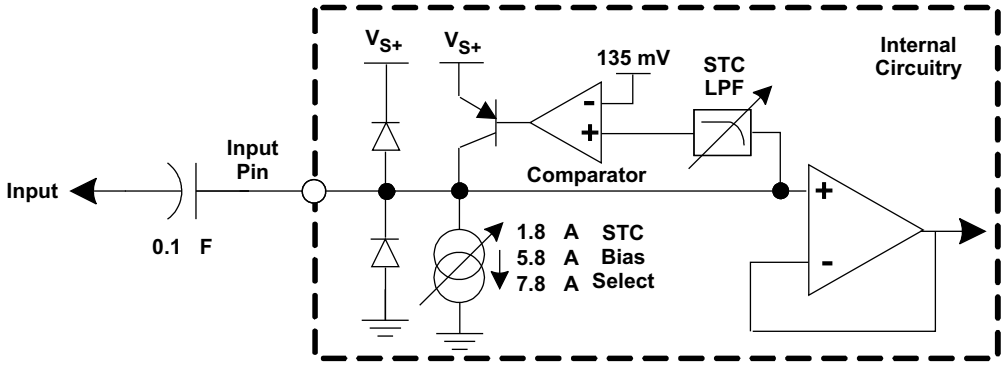


Figure 63. Equivalent AC Sync Tip Clamp Input Mode Circuit

APPLICATION INFORMATION (continued)

When the ac sync-tip-clamp (STC) operation is used, there must also be some finite amount of discharge bias current. As previously described, if the input signal goes below the 135-mV clamp level, the internal loop of the THS7303 sources current to increase the voltage appearing at the input pin. As the difference between the signal level and the 135-mV reference level increases, the amount of source current increases proportionally – supplying up to 2-mA of current. Thus the time to re-establish the proper STC voltage can be very fast. If the difference is small, then the source current is also small to account for minor voltage droop.

But, what happens if the input signal goes above the 135-mV input level? The problem is the video signal is always above this level and must not be altered in any way. But, if the sync level of the input signal is above the 135-mV level, then the internal discharge (sink) current reduces the ac-coupled bias signal to the proper 135-mV level.

This discharge current must not be large enough to alter the video signal appreciably or picture quality issues may arise. This is often seen by looking at the tilt (droop) of a constant luma signal being applied, and looking at the resulting output level. The associated change in luma level from the beginning of the video line to the end of the video line is the amount of line tilt (droop). The amount of tilt can be seen by the general formula:

$$I = C\ dV/dt$$

where I is the discharge current and C is the external coupling capacitor which is typically 0.1 μF. If the current (I) and the capacitor (C) are constant, then the tilt is governed by:

$$i/C = dV/dt$$

If the discharge current is small the amount of tilt is low which is good. But, the amount of time for the system to capture the sync signal could be too long. This is also termed *hum* rejection. Hum arises from the ac line voltage frequency of 50 Hz or 60 Hz. The value of the discharge current and the ac-coupling capacitor combine to dictate the hum rejection and the amount of line tilt.

Because many users have different thoughts as to the proper amount of hum rejection and line tilt, the THS7303 has incorporated a variable sink bias current selectable through the I^2C interface. The Low Bias mode selects about 1.8-μA of dc sink bias current for low line tilt. But, if more hum rejection is desired, then selecting the Mid Bias mode increases the dc sink bias current to about 5.8 μA. For severe environments, the High Bias mode has about 7.8 μA of dc sink bias current. This drawback to these higher bias modes is an increase in line tilt, but with an increase in hum rejection. The other method to change the hum rejection and line tilt is to change the input capacitor used. An increase in the capacitor from 0.1 μF to 0.22 μF decreases the hum rejection and line tilt by a factor of 2.2. A decrease of this input capacitor accomplishes the opposite effect. Note that the amplifier input bias current of nominally 0.6 μA has already been taken into account when stipulating the 1.8 μA/5.8 μA/7.8 μA current sink values.

To ensure proper stability of the AC STC control loop, the source impedance must be less than 600-Ω and the input capacitor must be greater than 0.01 μF. Otherwise, there is a possibility of the control loop ringing. The ringing appears on the output of the THS7303. Similar to the dc modes of operation, many DACs and encoders use a resistor to establish the output voltage. These resistors are typically less than 300 Ω. Thus, stability of the AC STC loop is ensured. But, if the source impedance looking from the THS7303 input perspective is high or open, then adding a 300-Ω resistor to GND ensures proper operation of the THS7303.

If a MUX channel is not required in the system, then it is recommended to place a 75-Ω resistor to GND. This is not required, but it helps minimize any potential issues.

OUTPUT MODES OF OPERATION – DC COUPLED

The THS7303 incorporates a rail-to-rail output stage that can be used to drive the line directly without the need for large ac-coupling capacitors. This is accomplished by connecting the output pin of each channel directly to the SAG output pin of the corresponding channel as shown in Figure 64. This offers the best line tilt and field tilt (or droop) performance since there is no ac coupling occurring. Keep in mind that if the input is ac coupled, then the resulting tilt due to the input ac coupling is still seen on the output regardless of the output coupling. The 70-mA output current drive capability of the THS7303 is designed to drive two video lines simultaneously – essentially a 75-Ω load – while keeping the output dynamic range as wide as possible.

One concern of dc coupling is if the line is terminated to ground. When the AC-bias input mode is selected, the output of the THS7303 is at mid-rail. With 2 lines terminated to ground, this creates a dc current path to exist which results in a slightly decreased high output voltage swing resulting in an increase in power dissipation of the

APPLICATION INFORMATION (continued)

THS7303. While the THS7303 is designed to operate with a junction temperature of up to 125°C, care must be taken to ensure that the junction temperature does not exceed this level or else long term reliability could suffer. Although this configuration adds less then 10 mW of power dissipation per channel, the overall low power dissipation of the THS7303 design minimizes potential thermal issues even when using the TSSOP package at high ambient temperatures.

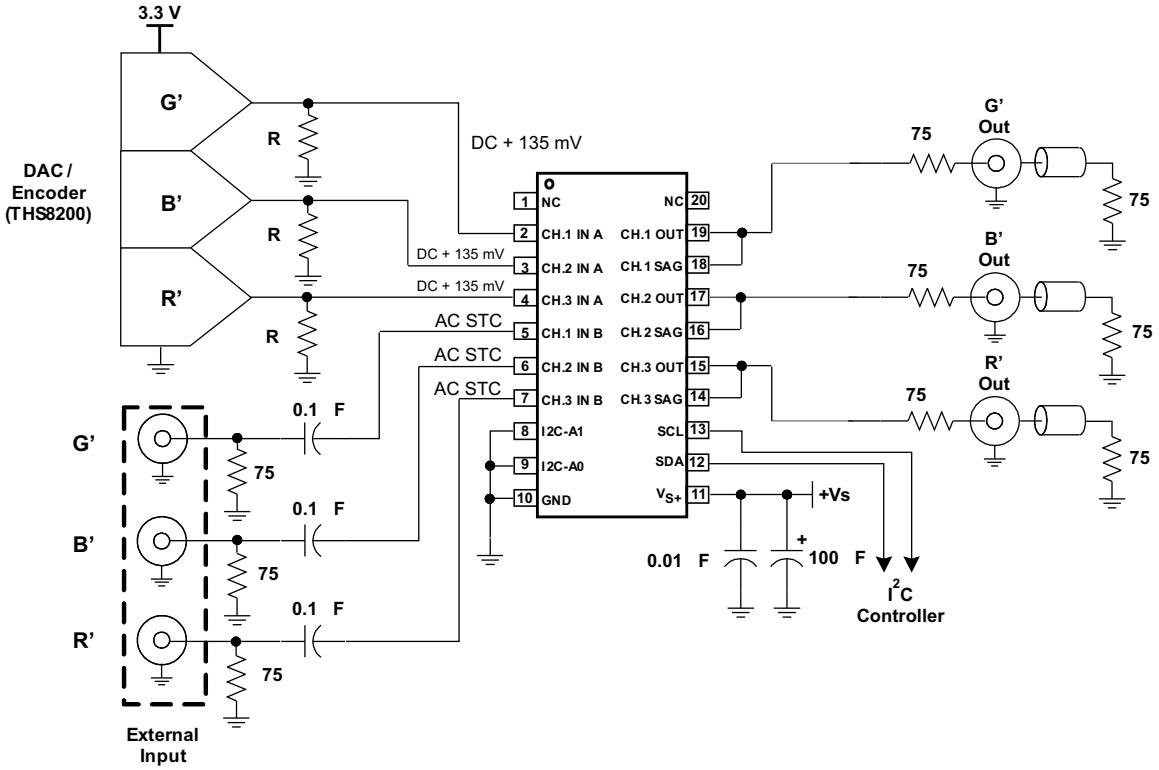


Figure 64. Typical G'B'R' (R'G'B') System With DC-Coupled Line Driving

Note that the THS7303 can drive the line with dc coupling regardless of the input mode of operation. The only requirement is to make sure the video line has proper termination in series with the output pin – typically 75-Ω. This helps isolate capacitive loading effects from the THS7303 output. Failure to isolate capacitive loads may result in instabilities with the output buffer potentially causing ringing or oscillations to appear. The stray capacitance appearing directly at the THS7303 output pins should be kept below 25-pF for best performance. When driving 2 video lines, each line should have its own 75-Ω source termination resistors to isolate the lines from each other.

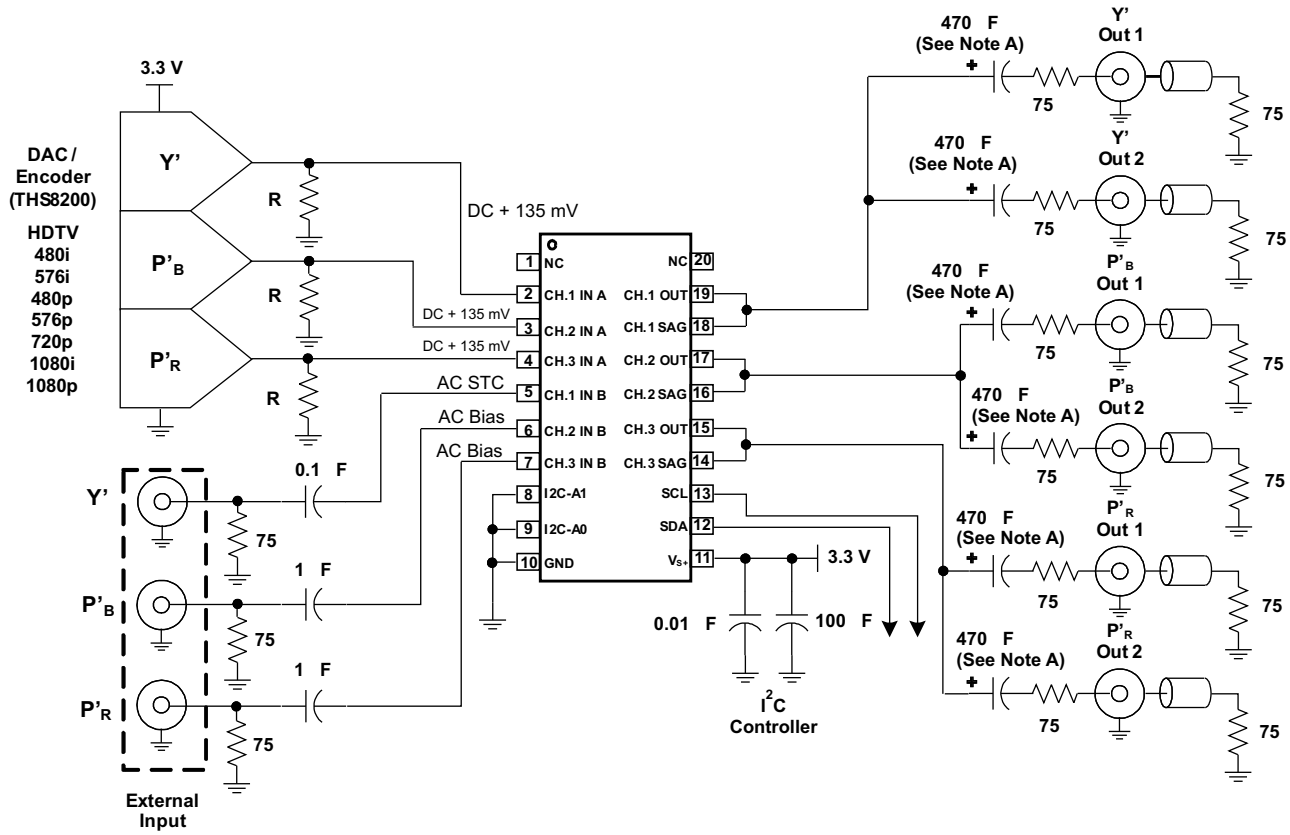
OUTPUT MODES OF OPERATION – AC COUPLED

The most common method of coupling the video signal to the line is by using a large capacitor. This capacitor is typically between 220 μF and 1000 μF, although 470 μF is most common. This value of this capacitor must be this large to minimize the line tilt (droop) and/or field tilt associated with ac coupling as described previously in this document. Just like the dc output configuration, connection of the output pin of each channel directly to the SAG output pin of the corresponding channel should be as close as possible to the output pins of the THS7303.

The most common reason ac coupling is used is to ensure full interoperability with the receiving video system. This eliminates possible ground loops. It also ensures that regardless of the reference dc voltage used on the transmit side, the receive side can re-establishes the dc reference voltage to its own requirements.

APPLICATION INFORMATION (continued)

As with the dc output mode of operation, each line should have a 75-Ω source termination resistor in series with the ac-coupling capacitor. If 2 lines are to be driven, it is best to have each line use its own capacitor and resistor rather than sharing these components as shown in Figure 65.This helps ensure line-to-line dc isolation and other potential problems. Using a single 1000-µF capacitor for 2-lines can be done, but there is a chance for ground loops and interference creation between the two receivers.



A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-µF capacitor in parallel with these large capacitors.

Figure 65. Typical Y'P'$_B$P'$_R$ System Driving 2 AC-Coupled Video Lines

Due to the edge rates and frequencies of operation, it is recommended – but not required – to place a 0.1-µF to 0.01-µF capacitor in parallel with the large 220-µF to 1000-µF capacitors. These large value capacitors are most commonly aluminum electrolytic. It is commonly known that these capacitors have significantly large equivalent series resistance (ESR), and their impedance at high frequencies is large due to the associated inductances involved with their construction. The small 0.1-µF to 0.01-µF capacitors help pass these high frequency (>1 MHz) signals with lower impedance than the large capacitors. This is especially true when HD and computer R'G'B' signals are being used. Their associated edge rates and frequency content can reach beyond 30-MHz for HD signals and can be over 100-MHz for R'G'B' signals – frequencies that typical aluminum electrolytic capacitors typically cannot pass effectively.

Although it is common to use the same capacitor values for all the video lines, the frequency bandwidth of the chroma signal in a S-Video system are not required to go as low or as high as the frequency of the luma channel. Thus, the capacitor values of the chroma line(s) can be smaller – such as 0.1 µF.

APPLICATION INFORMATION (continued)

OUTPUT MODES OF OPERATION – AC COUPLED WITH SAG CORRECTION

Other than the line droop issue, ac coupling has another potential issue – size and cost. A 330-µF to 1000-µF capacitor is large and can be quite costly in a system. Multiply these items by the number of channels, and the size and costs can be significant. But, it is still desirable to use ac coupling to eliminate ground loop issues and insure interoperability among video devices.

The SAG nomenclature represents signal amplitude gain correction in this document. SAG correction is a method which is used to ac couple the video signal while using much smaller value capacitors. SAG correction is accomplished by manipulating the feedback network of the output buffer. The THS7303 was designed to take advantage of this compensation scheme while minimizing the number of external components required. Figure 66 shows the basic configuration of the output buffer stage along with the SAG configuration driving a single video line.

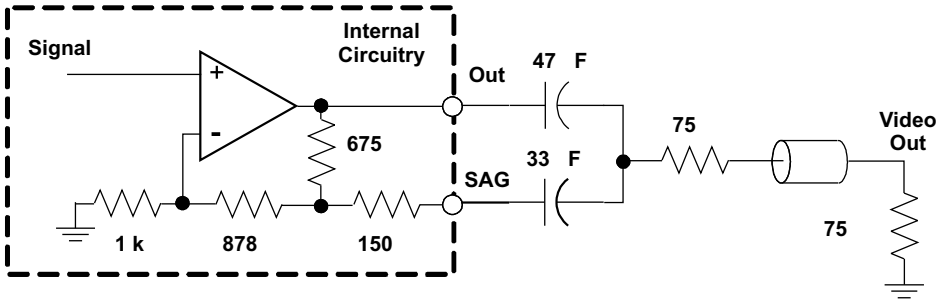


Figure 66. THS7303 Output Buffer Using SAG Corrected AC-Coupling

SAG compensation can be analyzed by looking at low frequency operation and high frequency operation. At low frequencies, the impedance of the capacitors are high and the corresponding gain of the amplifier is:

$$1 + \left(\frac{(675 + 878)}{1k}\right) = 2.55\ V/V\ (+\ 8.1\ dB). \quad (1)$$

But, at high frequencies, the impedance of the capacitors are low and the resulting gain of the amplifier is:

$$1 + \left(\frac{\left[(675 \parallel 150) + 878\right]}{1k}\right) = 1 + \left(\frac{1k}{1k}\right) = 2\ V/V\ (+\ 6.0\ dB) \quad (2)$$

which is needed to counter-act the doubly terminated 75-Ω output divider (-6 dB) circuit. Resulting in the video out signal equaling the Input signal amplitude.

When the SAG output pin is connected directly to the amplifier output, as found in the dc-coupled and the ac-coupled configurations, the gain is configured properly at 2 V/V (6 dB). The SAG pin is part of the negative feedback network. Thus, the capacitors and traces should be constructed as close as possible to the THS7303 to minimize parasitic issues. Failure to do so may result in ringing of the video signal.

If these large capacitors must be placed further than 15 mm away from the THS7303, it is recommended that a 0.01-µF capacitor be placed between the output of the channel and the SAG pin. This capacitor should be placed as close as possible to the THS7303 to minimize stray capacitance and inductance issues. Since SAG correction targets the low frequency operation area, there is no drawback of adding this high frequency capacitor to the circuit.

When SAG correction is used, low frequency gain is higher than the high frequency gain (8.1 dB vs. 6 dB). This gain counter acts the attenuation of the signal due to the increase in the 47-µF capacitor impedance. This amplifier gain increase is determined by the 33-µF capacitor (and associated internal resistor values) and causes a *Q* enhancement to occur at low frequencies – typically at about 15-Hz. The ratio of these capacitors determines the frequency and amplitude of this enhancement.

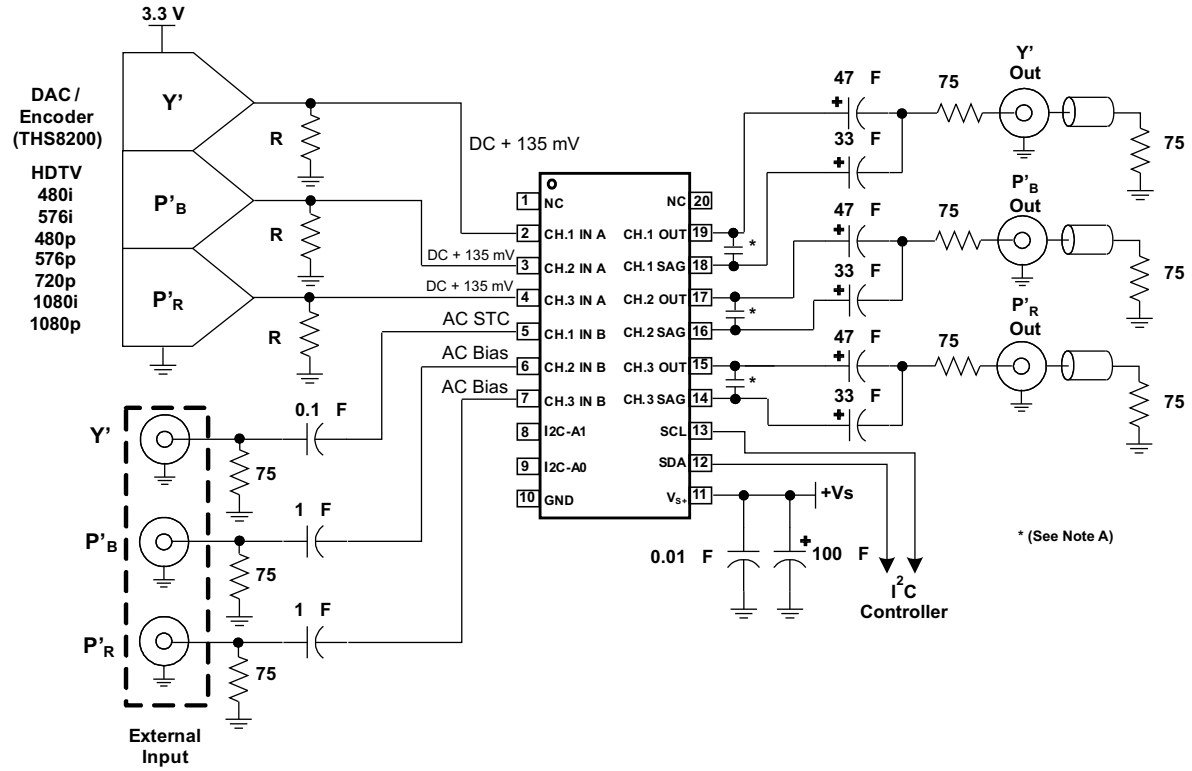
APPLICATION INFORMATION (continued)

The internal resistor values were chosen to optimize the system while using the 47-µF and 33-µF capacitors and to approximate the performance of a single 330-µF capacitor. These capacitors can be a different value if desired, but the characteristics of the system are altered accordingly. For example, if 22-µF capacitors is used for both sections, then there are increases in line tilt and field tilt. But, for some systems this may be considered acceptable such as 720p Y' signals with the associated faster line rates. Using larger values, such as 68 µF and 47 µF respectively, decreases field time distortion even further approaching performance of a single 470-µF capacitor.

It is important to note that the dc gain is about 2.55 V/V. Thus, if the input has a dc bias, the output dc bias is 2.55 times the input. For example, this results in an output bias point of 355 mV for the dc + 135 mV shift. Additionally, if the ac bias input mode is selected, the dc operating point is Vs/4 X 2.55, or 2.1 V with 3.3-V supply and 3.2 V with 5-V supply. This additional offset should not hinder the performance of the THS7303 as there is still plenty of voltage headroom between the dc operating point and the rail-to-rail output capability.

One possible concern about this configuration is the low frequency gain enhancement may cause saturation of the signal when low power supply voltages - such as 3 V - are used. Thus, the internal resistors were chosen to minimize the low frequency gain such that saturation is minimized. Other SAG correction parts have much higher low frequency gain (10 dB or higher), which when coupled with low power supply voltages, can easily create clipping on the output of the amplifier both dynamically and at dc. Other SAG correction parts do not use a resistor in series with the SAG pin. Neglecting this resistor can result in a large *Q* enhancement causing possible saturation issues. These systems typically require much larger capacitor values to minimize this problem which ultimately minimizes the benefits of SAG correction.

Figure 67 shows a SAG corrected configuration for the THS7303. If a S-Video chroma channel is being configured, there is no reason for SAG correction as the coupling capacitor is typically small at 0.1 µF. Thus, tying the output pin directly to the SAG output pin is recommended along with a 0.1-µF capacitor.



A. If the SAG correction capacitors are more than 15 mm from the THS7313, add a 0.01µF capacitor as shown.

Figure 67. Typical Y'P'$_B$P'$_R$ System Driving SAG Corrected AC-Coupled Video Lines

APPLICATION INFORMATION (continued)

LOW PASS FILTER AND BYPASS MODES

Each channel of the THS7303 incorporates a 5th-Order Low Pass Filter. These video reconstruction filters minimize DAC images from being passed onto the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems due to aliasing of the ADC. Another benefit of the filter is to smooth out aberrations in the signal which some DACs can have if their own internal filtering is not good. This helps with picture quality and helps insure the signal meets video bandwidth requirements.

Each filter has a Butterworth characteristic associated with it. They have been modified with a slightly lower *Q* than the traditional *Q* associated with the Butterworth response. The benefit of the Butterworth response is the frequency response is flat with a relatively steep initial attenuation at the corner frequency. The problem is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in frequency. An increase in group delay corresponds to a time domain pulse response that has overshoot and some possible ringing associated with the overshoot.

The use of other type of filters such as elliptic or chebyshev are not recommended for video applications due to their very large group delay variations near the corner frequency resulting in significant overshoot and ringing. While these elliptic or chebyshev filters may help meet the video standard specifications with respect to amplitude attenuation, their group delay is well beyond the standard specifications. Couple this with the fact that video can go from a white pixel to a black pixel over and over again, ringing occurs. Ringing typically causes a display to have *ghosting* or *fuzziness* appear on the edges of a sharp transition. However, a Bessel filter has ideal group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Thus the Butterworth filter is a respectable compromise for both attenuation and group delay.

The THS7303 filter has a slightly lower group delay variation near the corner frequency compared to an ideal Butterworth filter. This results in a time domain pulse response which still has some overshoot, but not as much as a true Butterworth filter. Additionally, the initial rate of attenuation in the frequency response is not as fast as an ideal Butterworth response, but it is an acceptable initial rate of attenuation considering the pulse and group delay characteristic benefits.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature changes. To minimize temperature effects, the THS7303 uses thin-film metal resistors and high quality - low temperature coefficient capacitors found in the BiCom-3 process. The filters have been specified by design to account for process variations and temperature variations to maintain proper filter characteristics. This maintains a low channel-to-channel time delay which is required for proper video signal performance.

The THS7303 filters have a nominal corner (-3 dB) frequency selectable at 9 MHz, 16 MHz, and 35 MHz along with a bypass mode. The 9-MHz filter is ideal for standard definition (SD) NTSC, PAL, and SECAM composite video (CVBS) signals. It is also useful for S-Video signals (Y'C'), 480i / 576i Y'P'$_B$P'$_R$, G'B'R', and Y'U'V' video signals. The -3-dB corner frequency was designed to be 9 MHz to allow a maximally flat video signal while achieving over 40-dB of attenuation at 27 MHz – a common frequency between the ADC 2nd and 3rd Nyquist zones found in many video receivers. This is important because any signal appearing around this frequency can appear in the baseband due to aliasing effects of an analog to digital converter found in a receiver.

The 9-MHz filter frequency was chosen to account for process variations in the THS7303. To ensure the required video frequencies are the least affected, the filter corner frequency must be high enough to allow for component variations. The other consideration is the attenuation must be large enough to ensure the anti-aliasing / reconstruction filtering meets the system demands. Thus, the selection of the filter frequencies was not chosen arbitrarily.

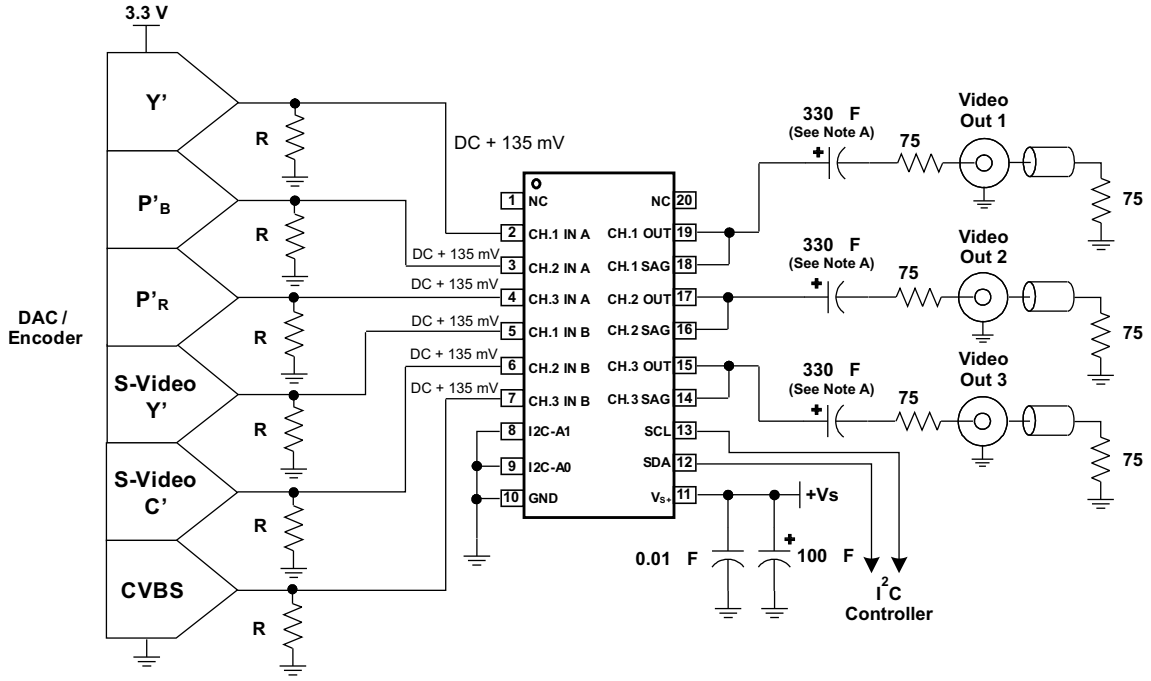
The 16-MHz filter was designed to pass 480p and 576p Y'P'$_B$P'$_R$ and G'B'R' video signals – sometimes referred as enhanced definition (ED). Additionally, this filter can be used to pass computer VGA signals with flat frequency response in the video spectrum. The 16-MHz filter can also be used for SD signals to ensure there is no amplitude aberration, and to have an exceptional low group delay within the SD video frequency range.

The 35-MHz filter is designed to pass high definition (HD) 720p and 1080i Y'P'$_B$P'$_R$ video signals along with G'B'R' (R'G'B') SVGA and XGA signals. If a 4:2:2 system is used, the P'$_B$P'$_R$ channels do not require the full bandwidth as required by the Y' channel. But, it is still recommended to use the same filter frequency of the Y' channel to match the group delay and timing of all 3 signals. Otherwise, extra delay compensation is required to minimize timing variations. This filter is also useful for passing 480p/576p signals with little amplitude or group delay variations within the ED frequency range.

APPLICATION INFORMATION (continued)

The THS7303 bypass mode has a 190-MHz bandwidth (-3 dB) and a 300 V/µs slewrate to pass G'B'R' (R'G'B') SXGA and UXGA signals with little degradation. This bypass mode is also useful for HDTV 1080p signals that require a 60-MHz video signal bandwidth.

The I^2C interface of the THS7303 allows each channel to be configured totally independent of the other channels. One of the benefits is that a multiple output encoder (or DAC) can be routed through one THS7303 with the proper input configuration and low-pass filter required regardless of the signal. This is useful for a portable system or in a low cost system where only one set (or 2 sets in parallel) is desired on the output of the system. An update of the I^2C commands changes the THS7303 channels. An example is shown in Figure 68 where the input MUX allows for one set of HDTV signals to be put into the THS7303, and then through an I^2C update, a SDTV set of signals is sent through the THS7303 with the proper input mode and low-pass filters.

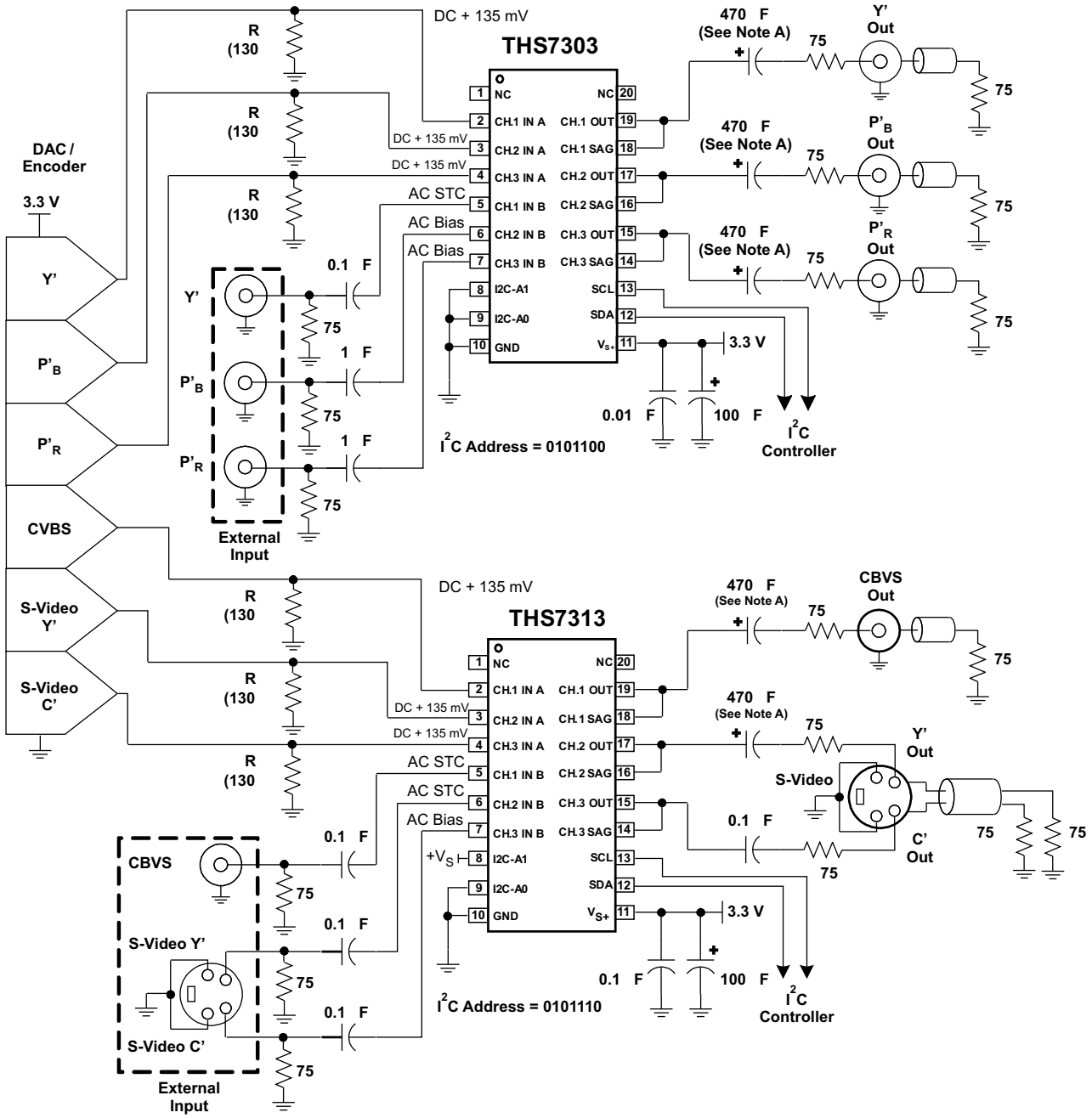


A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-µF capacitor in parallel with these large capacitors.

Figure 68. Typical SD/ED/ and HD Video and SDTB Encoder DAC Driving a Single THS7303

Although the circuit of Figure 68 conserves space and cost, the reuse of the output connections may not be the best solution. For a complete 6-channel system, it is better to use the THS7303 and the THS7313 (see SLOS483) together as shown in Figure 69. The THS7313 is targeted for SDTV signals and is limited to an 8-MHz filter. As the I^2C section discusses, it is easy to have both parts in one system as the I^2C address of each part can be one of 4 discrete addresses by the logic appearing on the I^2C-A1 and I^2C-A0 lines.

APPLICATION INFORMATION (continued)



A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-μF capacitor in parallel with these large capacitors.

Figure 69. Typical 6-Channel SDTV/EDTV/HDTV Encoder Interfacing to a THS7303 and a THS7313

I²C INTERFACE NOTES

The I²C interface is used to access the internal registers of the THS7303. I²C is a two-wire serial interface developed by Philips Semiconductor (see the I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The

APPLICATION INFORMATION (continued)

master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device. The THS7303 works as a slave and supports the standard mode transfer (100 kbps) and fast mode transfer (400 kbps) as defined in the I^2C-Bus specification. The THS7303 has been tested to be fully functional but not guaranteed with the high-speed mode (3.4 Mbps).

The basic I^2C start and stop access cycles are shown in Figure 70.

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

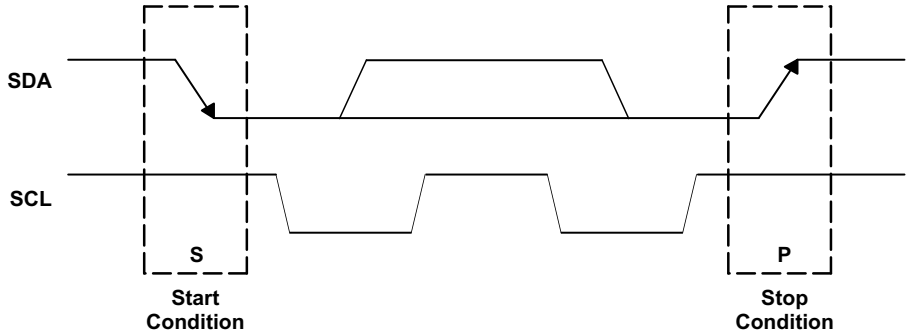


Figure 70. I^2C Start and Stop Conditions

GENERAL I^2C PROTOCOL

- The master initiates data transfer by generating a start condition. The start condition exist when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 70. All I^2C-compatible devices should recognize a start condition.
- The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 71). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 72) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (See Figure 73).
- To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 70). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

APPLICATION INFORMATION (continued)

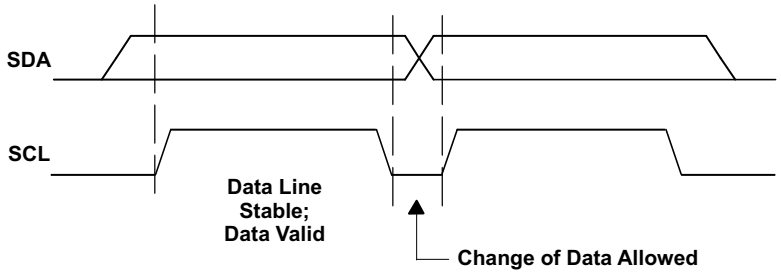


Figure 71. I²C Bit Transfer

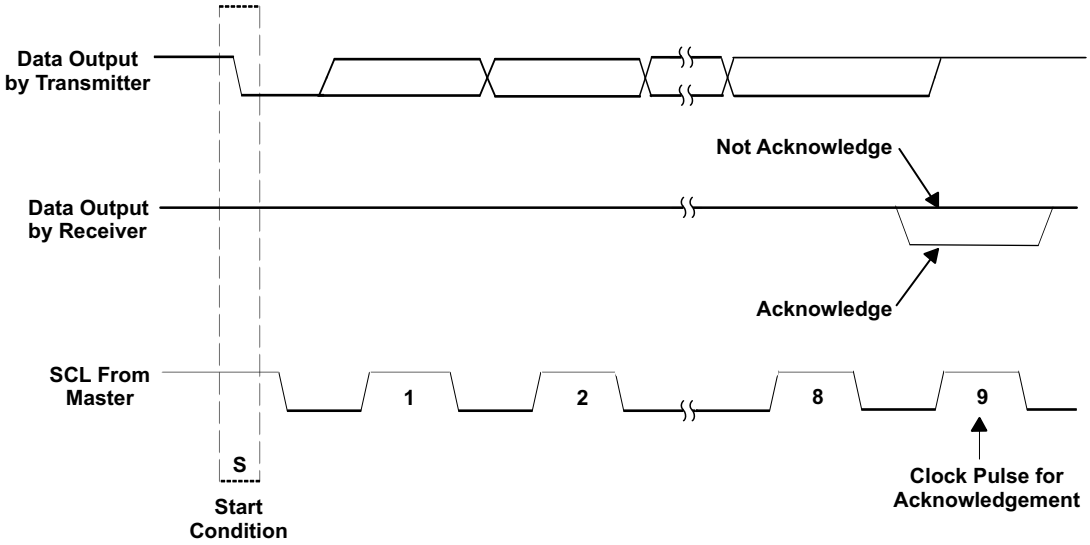


Figure 72. I²C Acknowledge

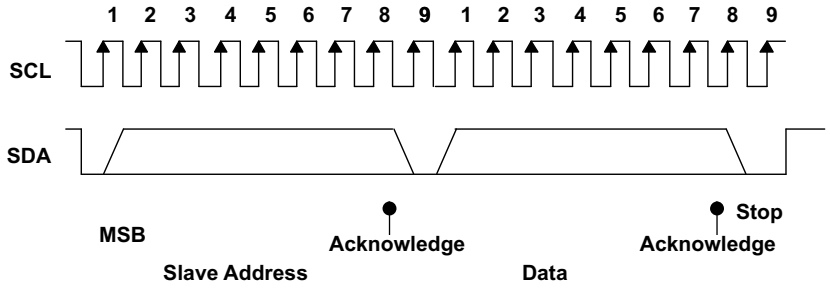


Figure 73. I²C Address and Data Cycles

During a write cycle, the transmitting device must not drive the SDA signal line during the acknowledge cycle, so that the receiving device may drive the SDA signal low. After each byte transfer following the address byte, the receiving device pulls the SDA line low for one SCL clock cycle. A stop condition is initiated by the transmitting device after the last byte is transferred. An example of a write cycle can be found in Figure 74 and Figure 75. Note that the THS7303 does not allow multiple write transfers to occur. See example section – Writing to the THS7303 for more information.

During a read cycle, the slave receiver acknowledges the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and

APPLICATION INFORMATION (continued)

acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge (A) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 76 and Figure 77. Note that the THS7303 does not allow multiple read transfers to occur. See example section – Reading from the THS7303 for more information.

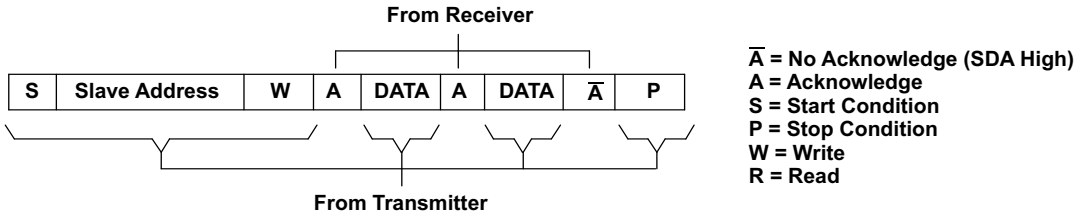


Figure 74. I²C Write Cycle

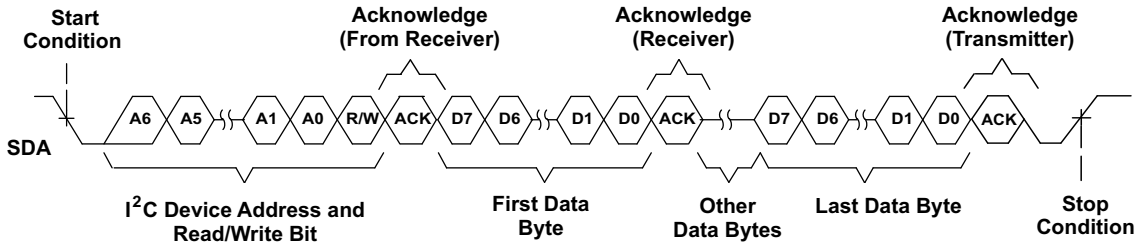


Figure 75. Multiple Byte Write Transfer

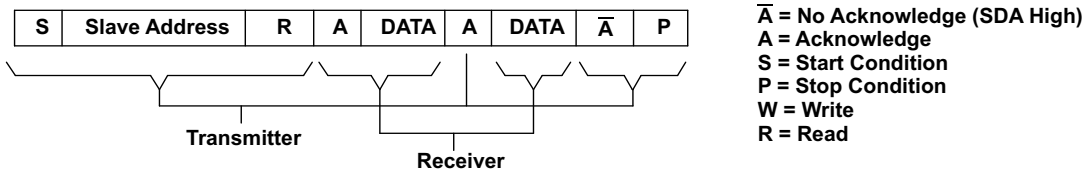


Figure 76. I²C Read Cycle

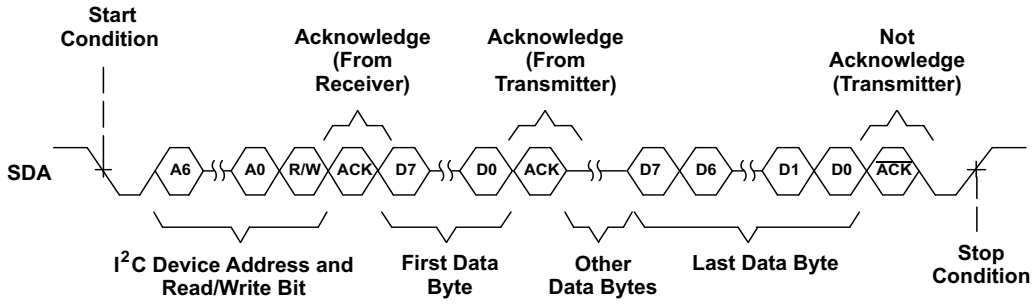


Figure 77. Multiple Byte Read Transfer

Slave Address

Both the SDA and the SCL must be connected to a positive supply voltage via a pullup resistor. These resistors should comply with the I²C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The first 5 Bits (MSBs) of the address are factory preset to 01011. The next two bits of the THS7303 address are

APPLICATION INFORMATION (continued)

controlled by the Logic levels appearing on the I^2C-A1 and I^2C-A0 pins. The I^2C-A1 and I^2C-A0 address inputs can be connected to V_{S+} for Logic 1, GND for Logic 0, or it can be actively driven by TTL/CMOS logic levels. The device address is set by the state of these pins and is not latched. Thus, a dynamic address control system can be used to incorporate several devices on the same system. Up to four THS7303 devices can be connected to the same I^2C-Bus without requiring additional glue logic. Table 1 lists the possible addresses for the THS7303

Table 1. THS7303 Slave Addresses

FIXED ADDRESS					SELECTABLE WITH ADDRESS PINS		READ/WRITE BIT
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 (A1)	Bit 1 (A0)	Bit 0
0	1	0	1	1	0	0	0
0	1	0	1	1	0	0	1
0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1
0	1	0	1	1	1	0	0
0	1	0	1	1	1	0	1
0	1	0	1	1	1	1	0
0	1	0	1	1	1	1	1

Channel Selection Register Description (Subaddress)

The THS7303 operates using only a single byte transfer protocol similar to Figure 74 and Figure 76. The internal subaddress registers and the functionality of each are found in Table 2. When writing to the device, it is required to send one byte of data to the corresponding internal subaddress. If control of all three channels is desired, then the master has to cycle through all the subaddresses (channels) one at a time, see the example section *–Writing to the THS7303* for the proper procedure of writing to the THS7303.

During a read cycle, the THS7303 sends the data in its selected subaddress (or channel) in a single transfer to the master device requesting the information. See the example section *–Reading from the THS7303* for the proper procedure on reading from the THS7303.

On power up, the THS7303 registers are in a random state from part-to-part. It remains in this random state until a valid write sequence is made to the THS7303. A total of 9 bytes of data completely configures all channels of the THS7303. As such, configuring the THS7303 should be done on power-up of the system. Note that one such random state (acknowledge state) can be engaged. To circumvent this state, have one SCL cycle run, and the acknowledge state disengages.

Table 2. THS7303 Channel Selection Register Bit Assignments

REGISTER NAME	BIT ADDRESS (b7b6b5....b0)
Channel 1	0000 0001
Channel 2	0000 0010
Channel 3	0000 0011

Channel Register Bit Descriptions

Each bit of the sub-address (channel selection) control register as described above allows the user to individually control the functionality of the THS7303. The benefit of this process allows the user to control the functionality of each channel independent of the other channels. The bit description is decoded in Table 3.

Table 3. THS7303 Channel Register Bit Decoder Table

BIT	FUNCTION	BIT VALUE(S)	RESULT
(MSB) 7, 6	STC Low Pass Filter Selection	0 0	500-kHz Filter – Useful for 9-MHz Video LPF
		0 1	2.5-MHz Filter – Useful for 16-MHz Video LPF
		1 0	5-MHz Filter – Useful for 35-MHz/Bypass Video LPF
		1 1	5-MHz Filter – Useful for 35-MHz/Bypass Video LPF
5	Input MUX Selection	0	Input A Select
		1	Input B Select
4 , 3	Low-Pass Filter Frequency Selection	0 0	9-MHz LPF – Useful for SDTV, S-Video, 480i/576i
		0 1	16-MHz LPF – Useful for EDTV 480p/576p and VGA
		1 0	35-MHz LPF – Useful for 720p, 1080i, and SVGA/XGA
		1 1	Bypass LPF – Useful for 1080p and SXGA/UXGA
2, 1, 0 (LSB)	Input Bias Mode Selection and Disable Control	0 0 0	Disable Channel – Conserves Power
		0 0 1	Channel On – Mute Function – No Output
		0 1 0	Channel On – DC Bias Select
		0 1 1	Channel On – DC Bias + 135 mV Offset Select
		1 0 0	Channel On – AC Bias Select
		1 0 1	Channel On – Sync Tip Clamp with Low Bias
		1 1 0	Channel On – Sync Tip Clamp with Mid Bias
		1 1 1	Channel On – Sync Tip Clamp with High Bias

Bits 7 (MSB) and 6 – Controls the AC-Sync Tip Clamp Low Pass Filter function. If AC-STC mode is not used, this function is ignored.

Bit 5 – Controls the input MUX of the THS7303.

Bits 4 and 3 – Controls the 5th order low pass filter –3 dB corner frequency or the bypass mode of operation.

Bits 2, 1, and 0 (LSB) – Selects the input biasing of the THS7303 and the power-savings function. When sync-tip clamp is selected, the dc input sink bias current is also selectable.

EXAMPLE – WRITING TO THE THS7303

The proper way to write to the THS7303 is illustrated as follows:

An I^2C master initiates a write operation to the THS7303 by generating a start condition (S) followed by the THS7303 I^2C address (as shown below), in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the THS7303, the master presents the subaddress (channel) it wants to write consisting of one byte of data, MSB first. The THS7303 acknowledges the byte after completion of the transfer. Finally the master presents the data it wants to write to the register (channel) and the THS7303 acknowledges the byte. The I^2C master then terminates the write operation by generating a stop condition (P). Note that the THS7303 does not support multi-byte transfers. To write to all three channels – or registers – this procedure must be repeated for each register one series at a time (i.e., repeat steps 1 through 8 for each channel).

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each X Logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either Vs+ or GND.

Step 3	9
I^2C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I²C Write Channel Address (Master)	0	0	0	0	0	0	Addr	Addr

Where Addr is determined by the values shown in Table 2.

Step 5	9
I²C Acknowledge (Slave)	A

Step 6	7	6	5	4	3	2	1	0
I²C Write Data (Master)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the values shown in Table 3.

Step 7	9
I²C Acknowledge (Slave)	A

Step 8	0
I²C Stop (Master)	P

For Step 6, an example of the proper bit control for selecting Input B of the MUX, a 720p Y' channel signal with AC-STC lowest line tilt and with the shortest sync filter is 1111 0101.

EXAMPLE – READING FROM THE THS7303

The read operation consists of two phases. The first phase is the address phase. In this phase, an I²C master initiates a write operation to the THS7303 by generating a start condition (S) followed by the THS7303 I²C address, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the THS7303, the master presents the sub-address (channel) of the register it wants to read. After the cycle is acknowledged (A), the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I²C master initiates a read operation to the THS7303 by generating a start condition followed by the THS7303 I²C address (as shown below for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the THS7303, the I²C master receives one byte of data from the THS7303. After the data byte has been transferred from the THS7303 to the master, the master generates a not acknowledge followed by a stop. Similar to the Write function, to read all channels Steps 1 through 11 must be repeated for each and every channel desired.

THS7303 Read Phase 1:

Step 1	0
I²C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I²C General Address (Master)	0	1	0	1	1	X	X	0

Where each X Logic state is defined by I²C-A1 and I²C-A0 pins being tied to either Vs+ or GND.

Step 3	9
I²C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I²C Read Channel Address (Master)	0	0	0	0	0	0	Addr	Addr

Where Addr is determined by the values shown in Table 2.

Step 5	9
I²C Acknowledge (Slave)	A

Step 6	0
I²C Start (Master)	P

THS7303 Read Phase 2:

Step 7	0
I^2C Start (Master)	S

Step 8	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	1

Where each X Logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either Vs+ or GND.

Step 9	9
I^2C Acknowledge (Slave)	A

Step 10	7	6	5	4	3	2	1	0
I^2C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the Logic values contained in the Channel Register.

Step 11	9
I^2C Not-Acknowledge (Master)	$\overline{A}$

Step 12	0
I^2C Stop (Master)	P

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
THS7303PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS7303PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS7303PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS7303PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

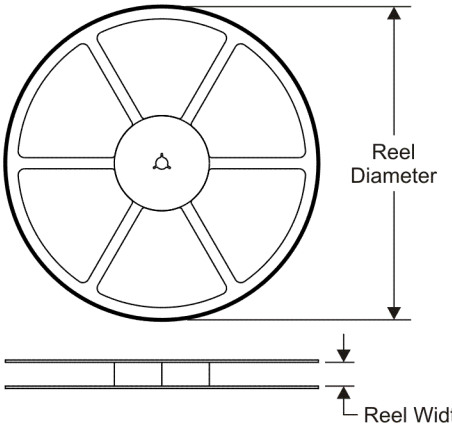
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

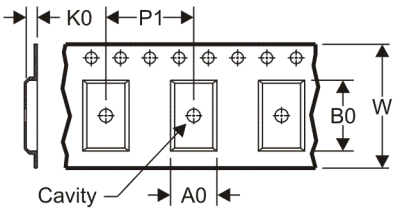
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

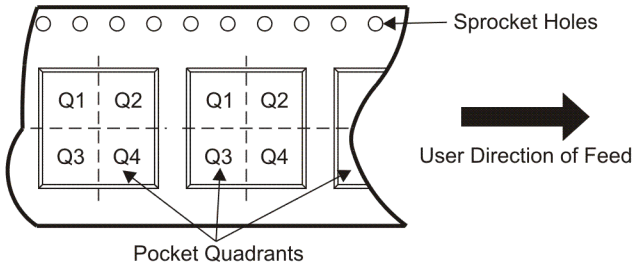


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

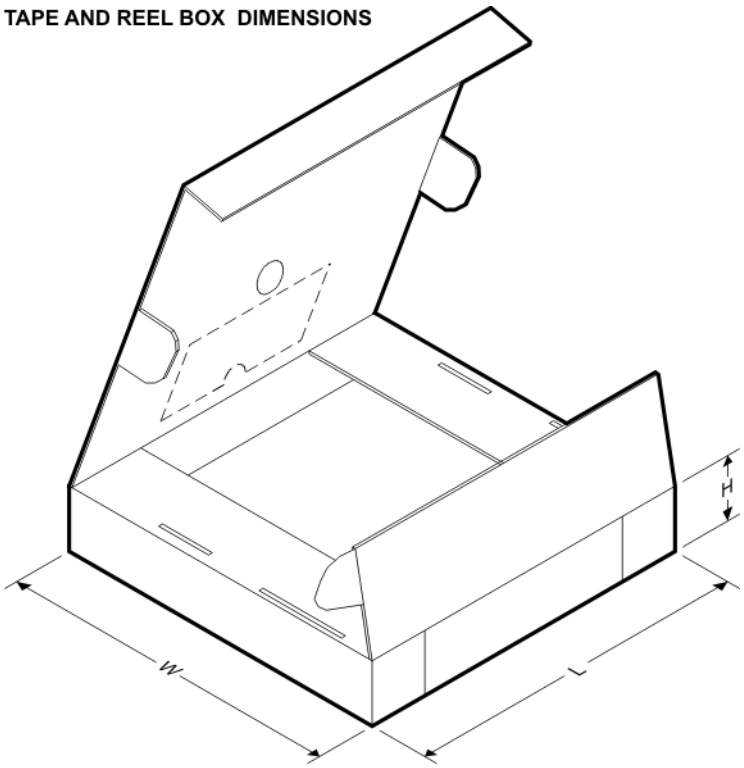
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7303PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

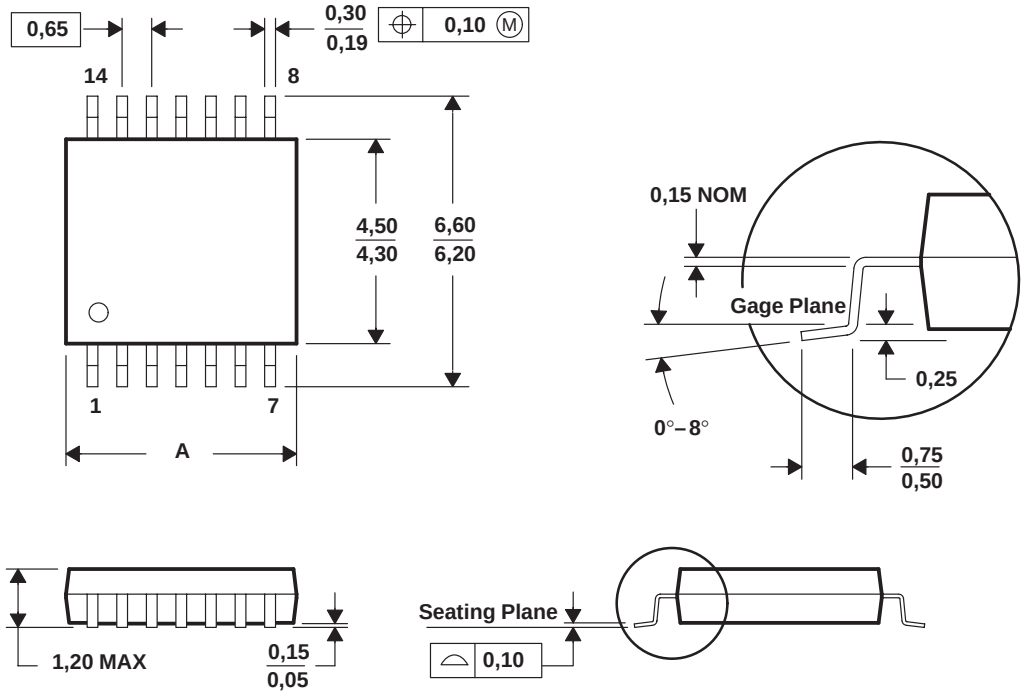


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7303PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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